FPGA Interfacing and Signal Processing

David Hawkins
(dwh@ovro.caltech.edu)
Caltech's Owens Valley Radio Observatory,
and CARMA.

Presentation

1. SZA/CARMA interferometers
2. FPGA interfacing
   - Control
   - Data
3. Signal processing
   - FPGA features
   - LFSRs, NCOs, FIR filters …
4. Control software

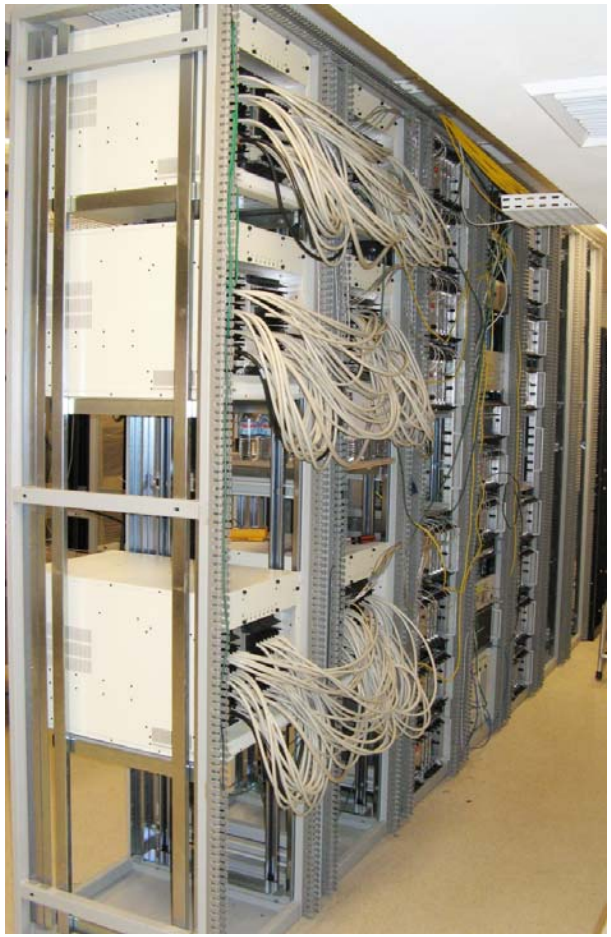
SZA Interferometer

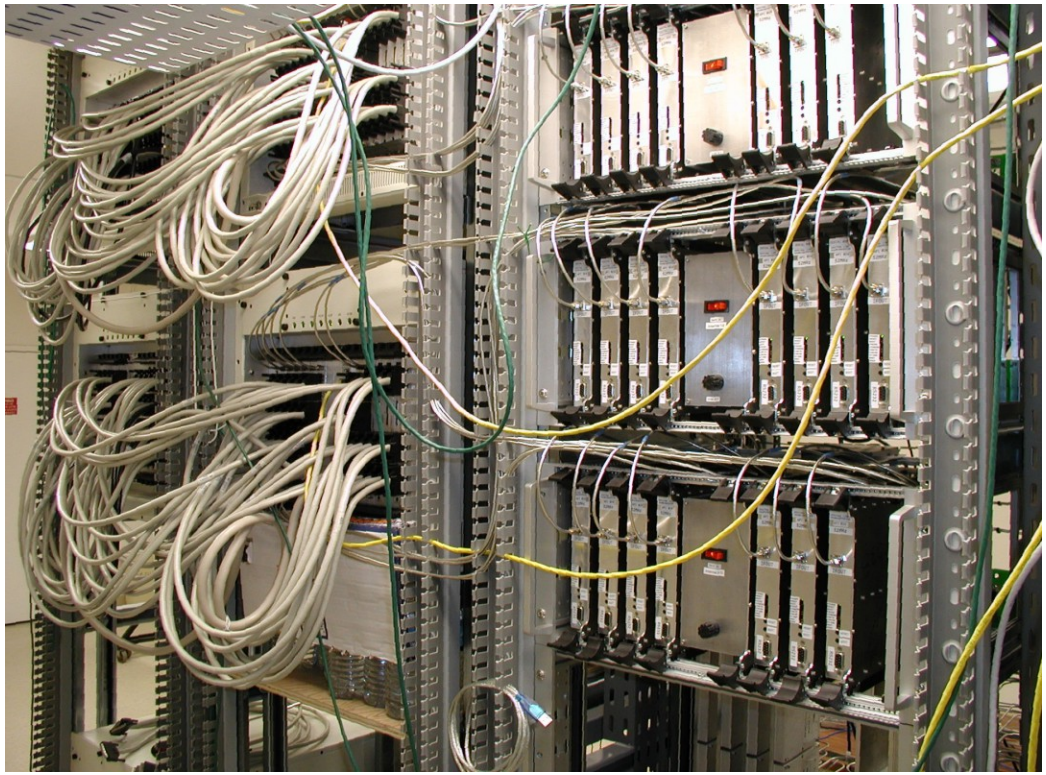
SZA Correlator

CARMA Interferometer

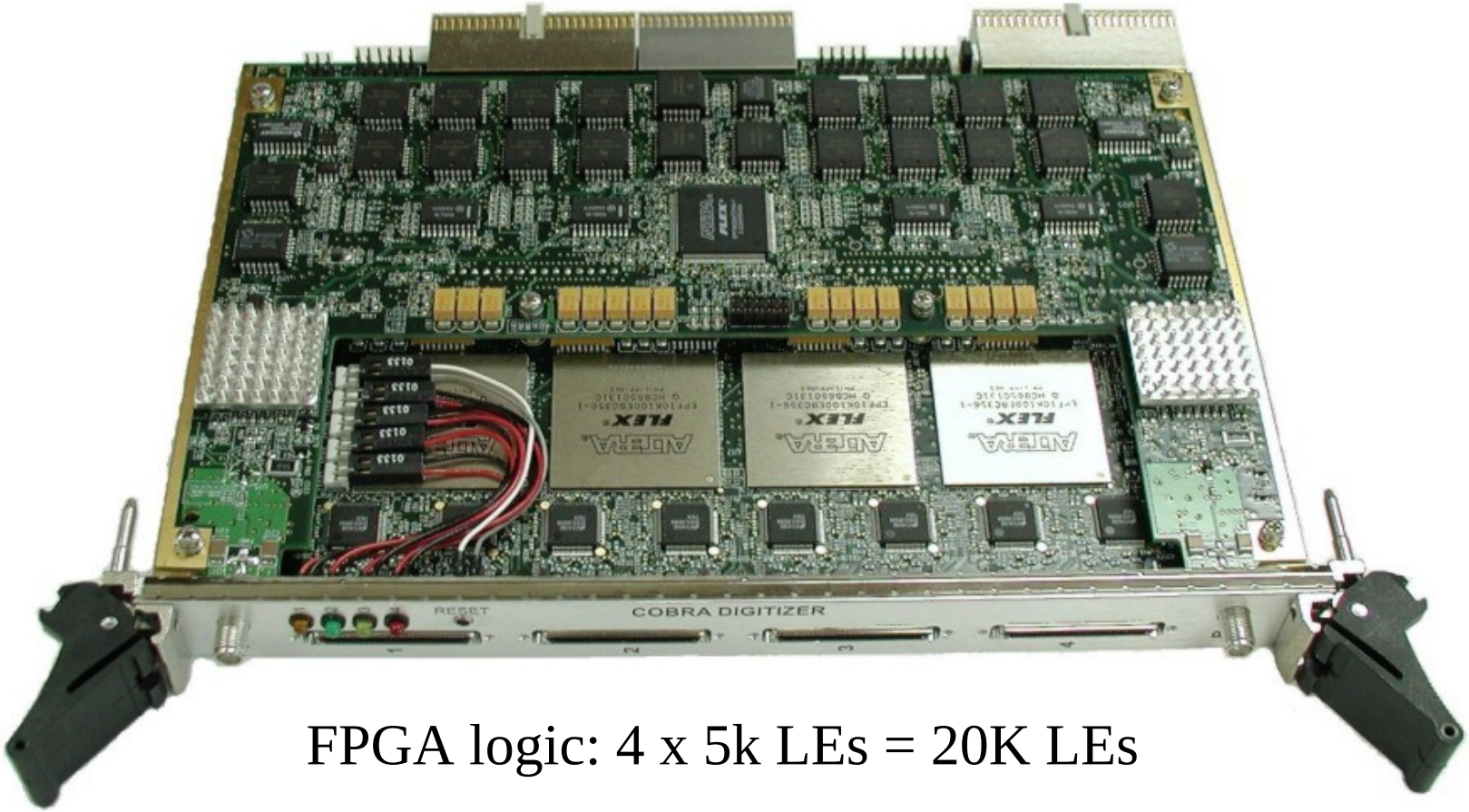
http://www.mmarray.org

CARMA Correlator



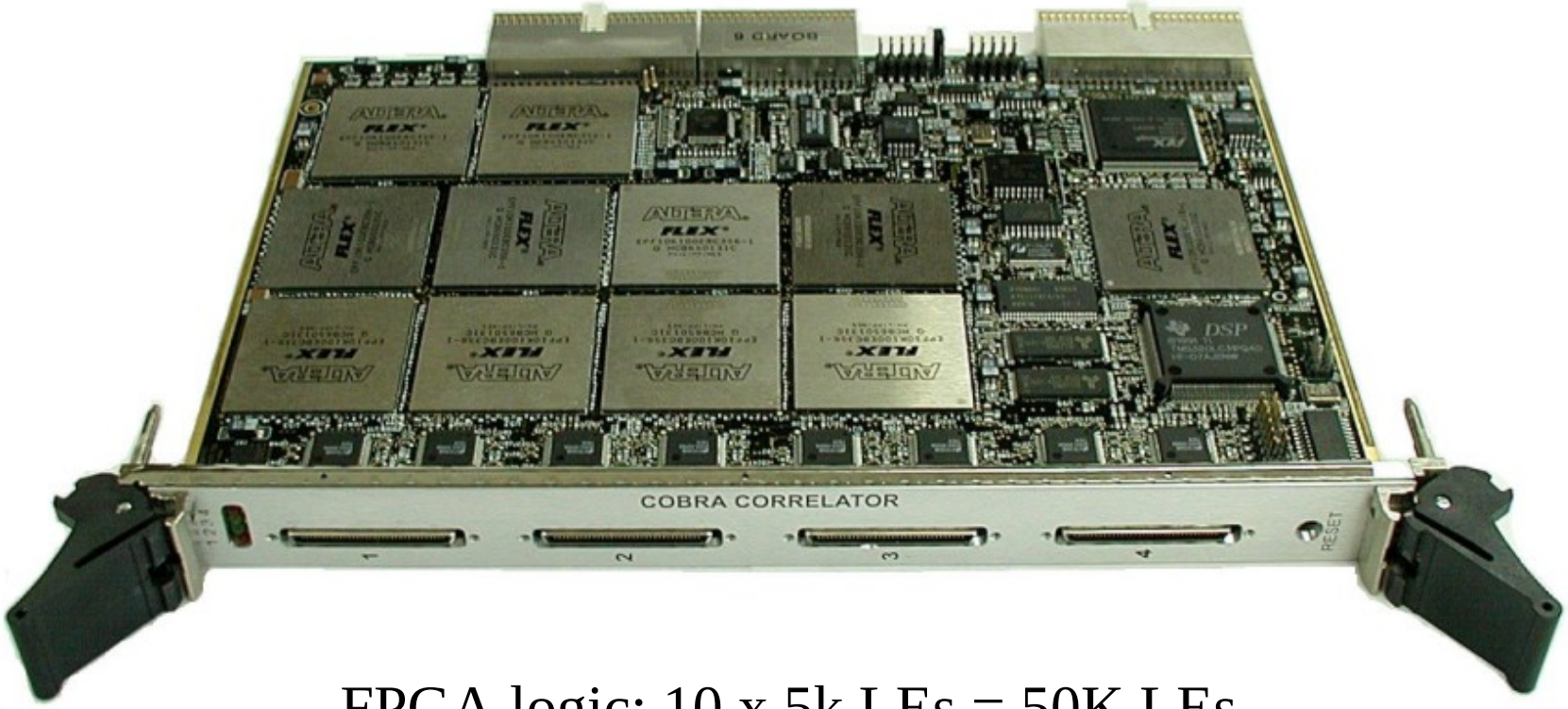


COBRA Digitizer Board



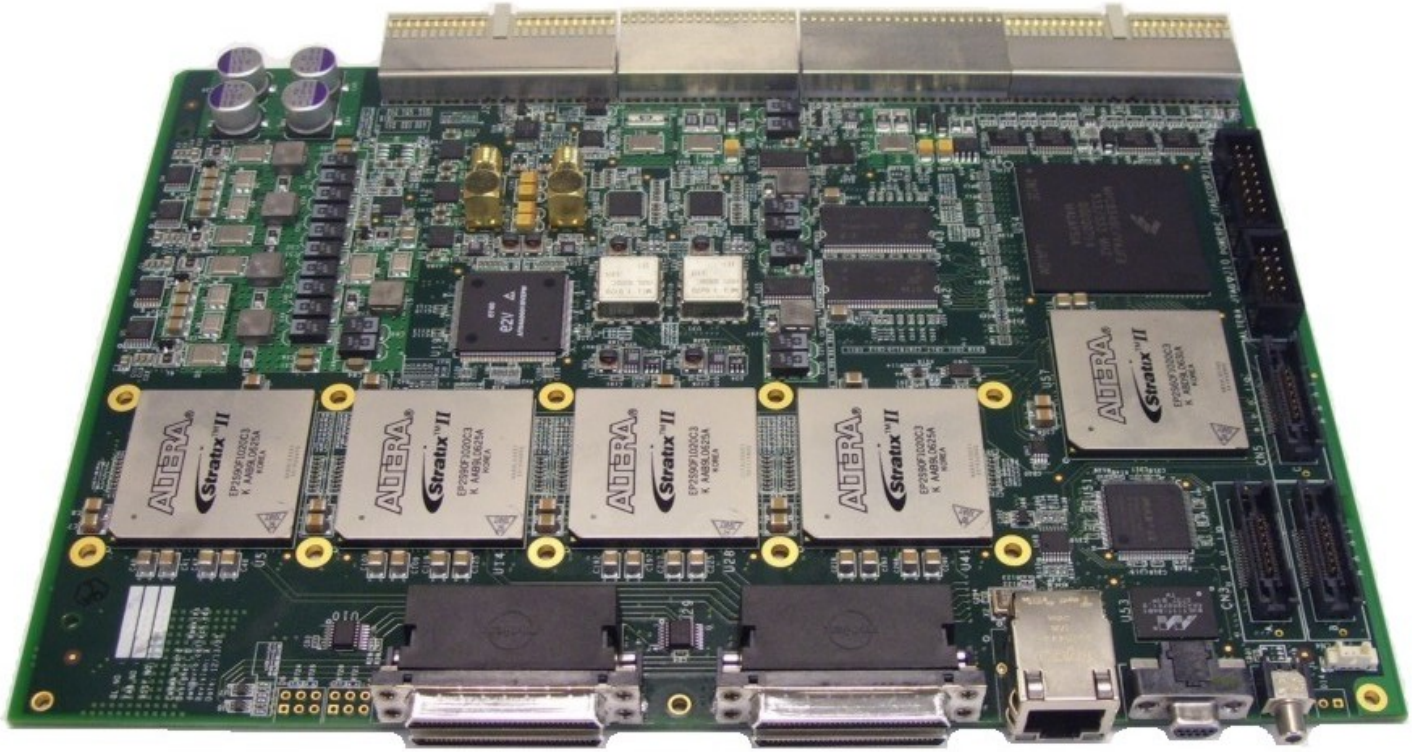
FPGA logic: 4 x 5k LEs = 20K LEs

COBRA Correlator Board



FPGA logic: 10 x 5k LEs = 50K LEs

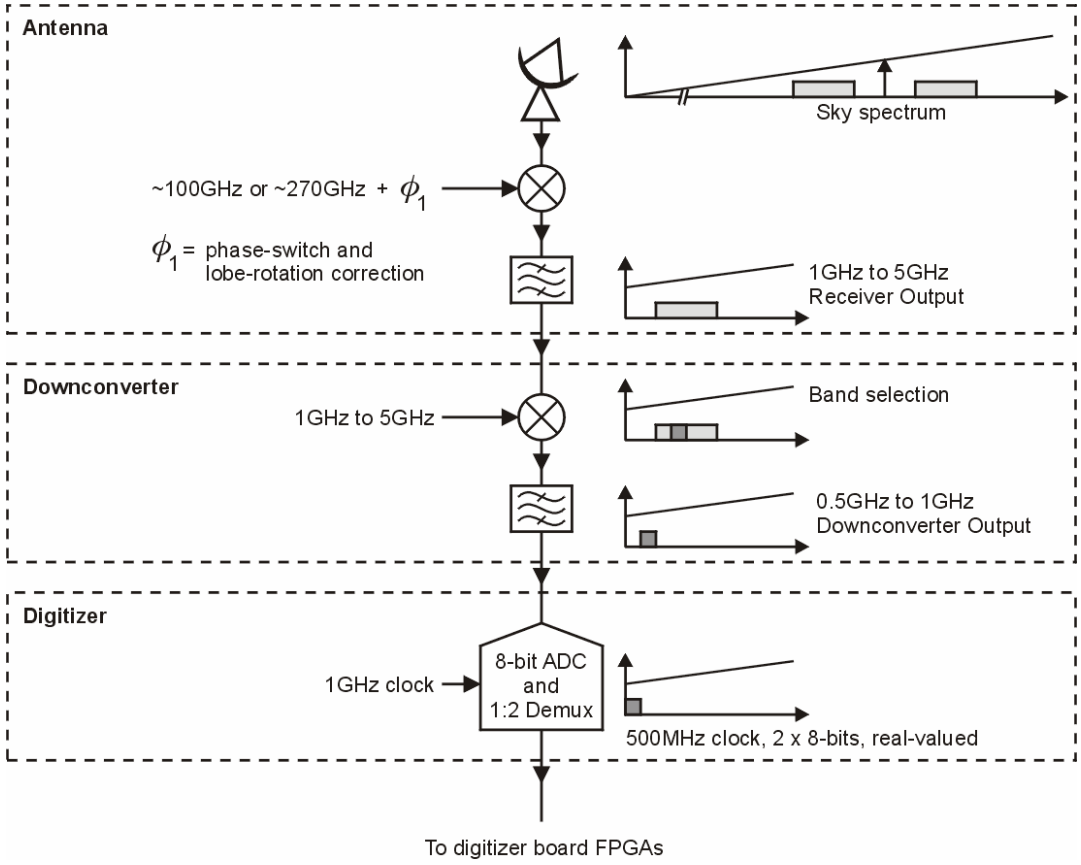
CARMA Digitizer/Correlator Board

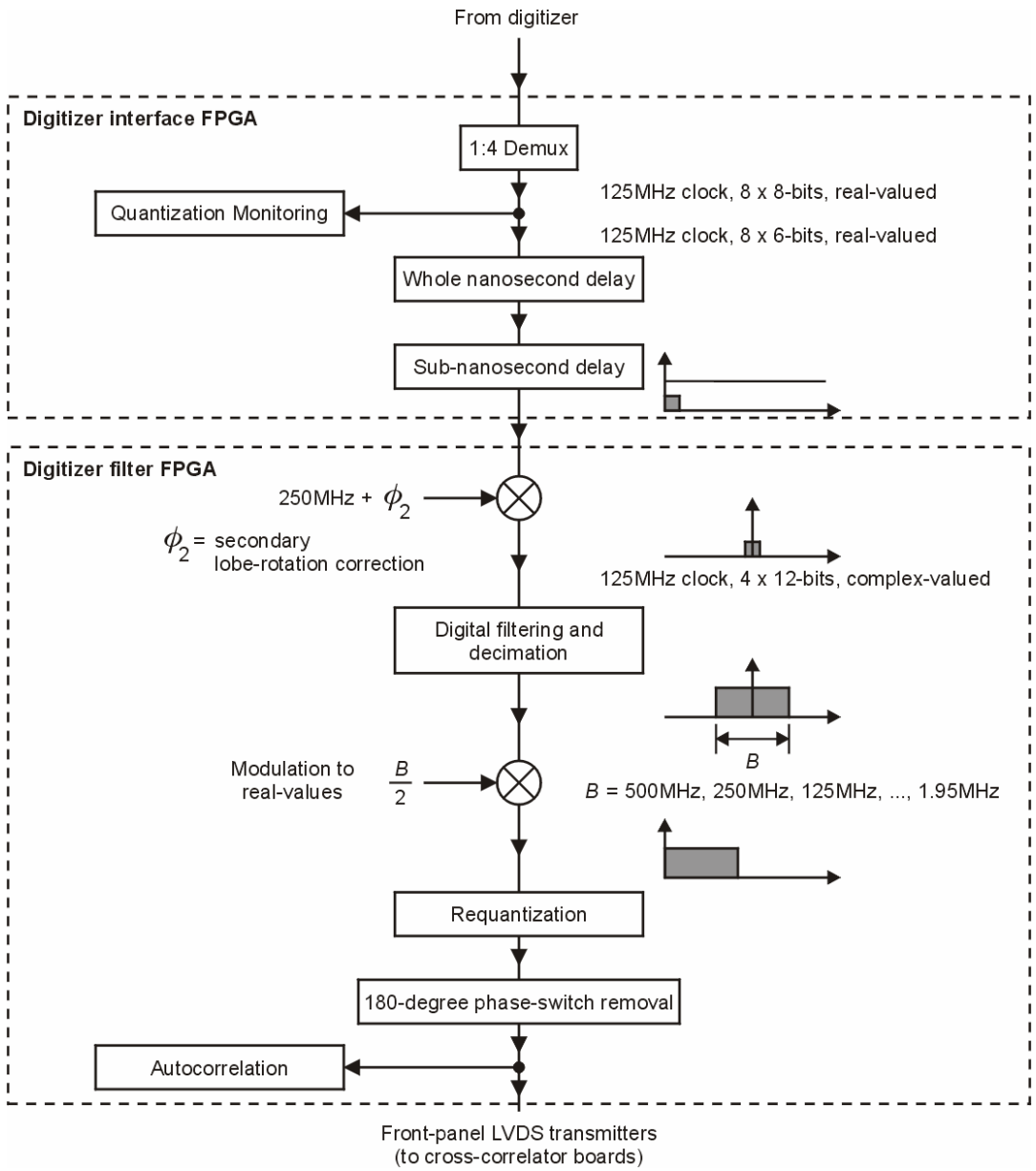


Digitizer FPGA logic: 4 x 90k LEs = 360K LEs

Correlator FPGA logic: 4 x 130k LEs = 520K LEs

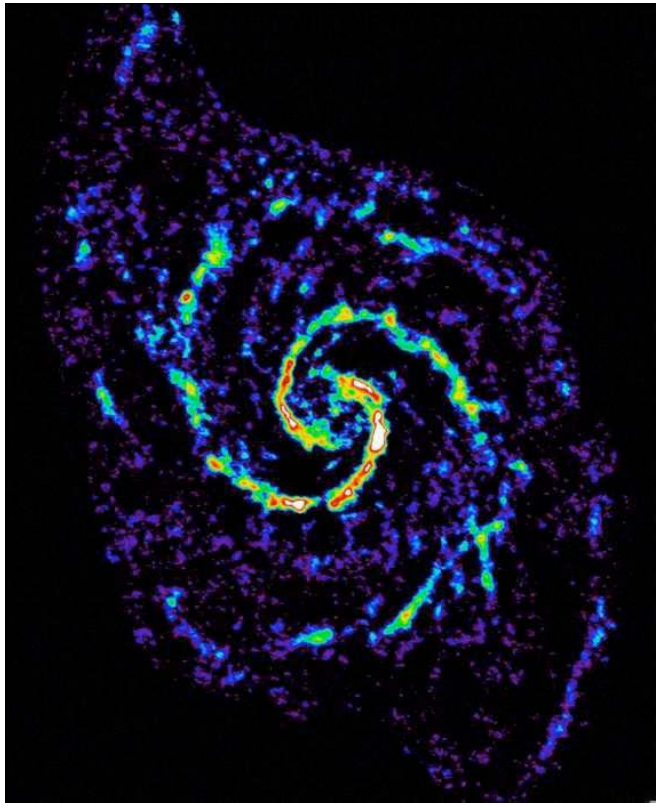
Antenna-based processing




From digitizer
Digitizer interface FPGA
1:4 Demux
Quantization Monitoring
125MHz clock, 8 x 8-bits, real-valued
125MHz clock, 8 x 6-bits, real-valued
Whole nanosecond delay
Sub-nanosecond delay
Digitizer filter FPGA
250MHz + ϕ_2
ϕ_2 = secondary lobe-rotation correction
125MHz clock, 4 x 12-bits, complex-valued
Digital filtering and decimation
B
Modulation to real-values
$\frac{B}{2}$
B = 500MHz, 250MHz, 125MHz, ..., 1.95MHz
Requantization
180-degree phase-switch removal
Autocorrelation
Front-panel LVDS transmitters
(to cross-correlator boards)

The Whirlpool Galaxy (M51)

(a) Hubble



(b) CARMA

FPGA Interfacing

- Control
  - Read/write traffic (single/block transfers)
  - Standardized interfaces; PCI, GbE
- Data
  - Continuous sample (streaming)
  - Device-specific interfaces; ADC, DAC

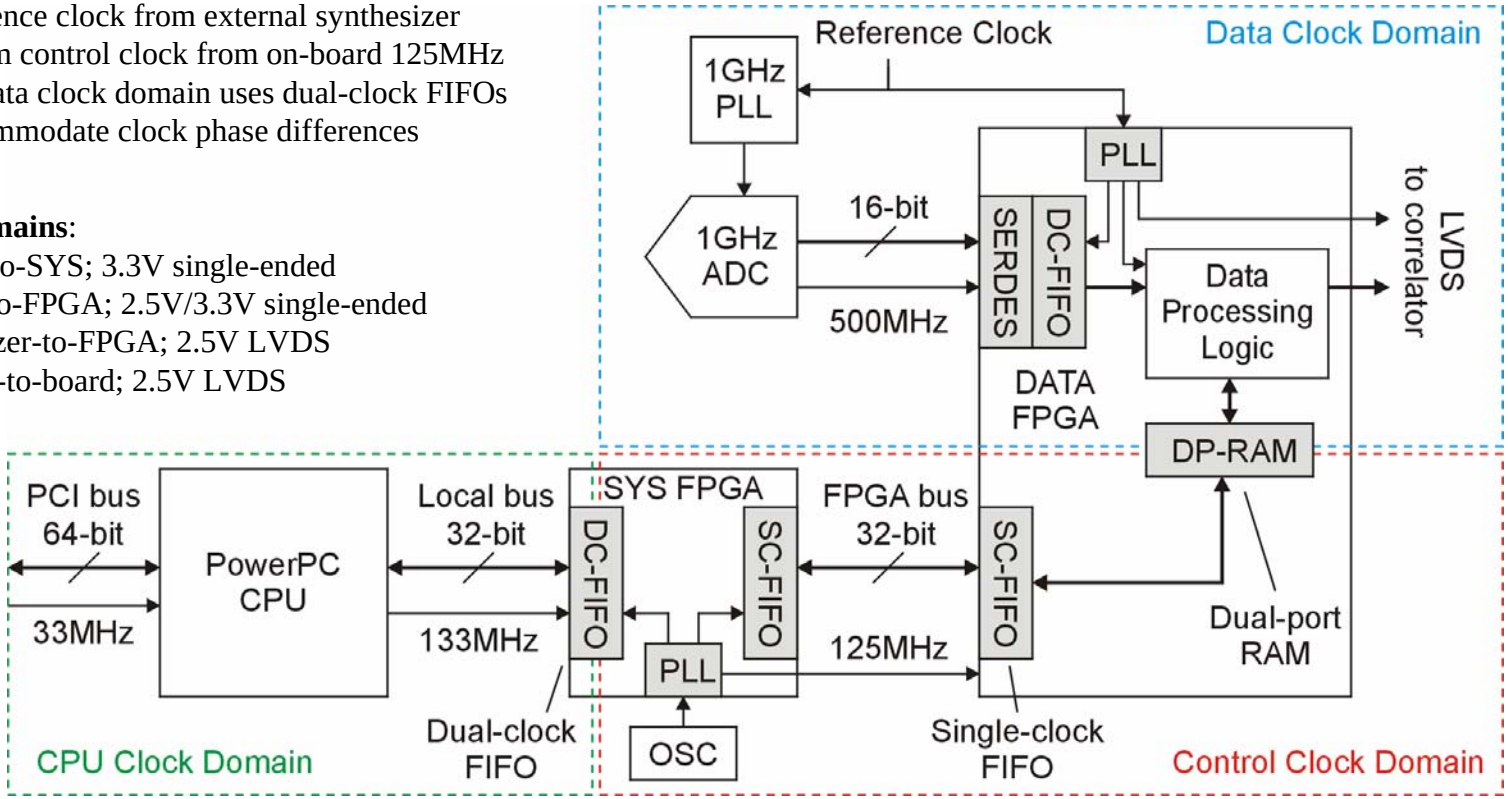
FPGA Interfacing; Features

- Standard IP cores;
  - PCI, PCI Express, GbE, DDR
- Flexible I/O interfaces;
  - LV/CMOS, LVDS, DDR
- Flexible clocking (PLLs)
- Vendor specific IP;
  - Single and dual-clock first-in, first-out, (FIFO) buffers
  - Single and dual-ported RAM
  - Phase-locked Loops
  - High-speed synchronous serializer/deserializer

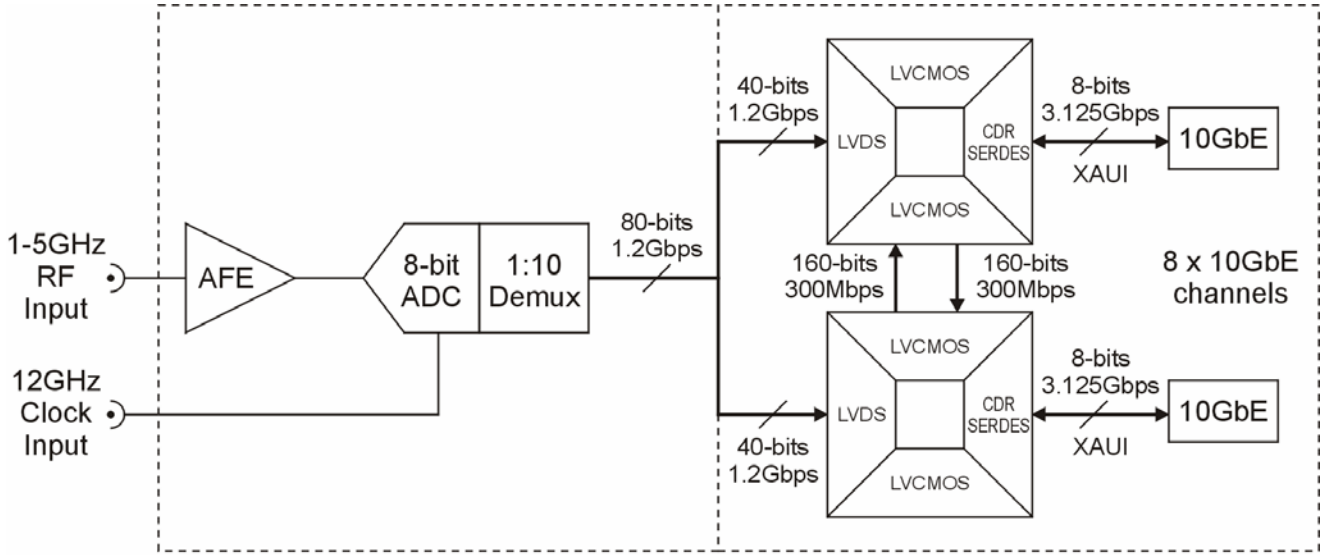
Example 1; CARMA board

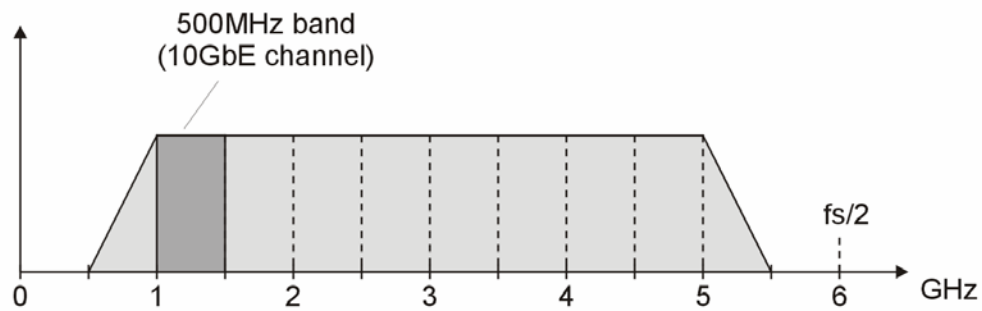
Clock domains:
- PCI clock from cPCI host CPU
- Reference clock from external synthesizer
- System control clock from on-board 125MHz
- The data clock domain uses dual-clock FIFOs to accommodate clock phase differences

I/O domains:
- CPU-to-SYS; 3.3V single-ended
- SYS-to-FPGA; 2.5V/3.3V single-ended
- Digitizer-to-FPGA; 2.5V LVDS
- Board-to-board; 2.5V LVDS



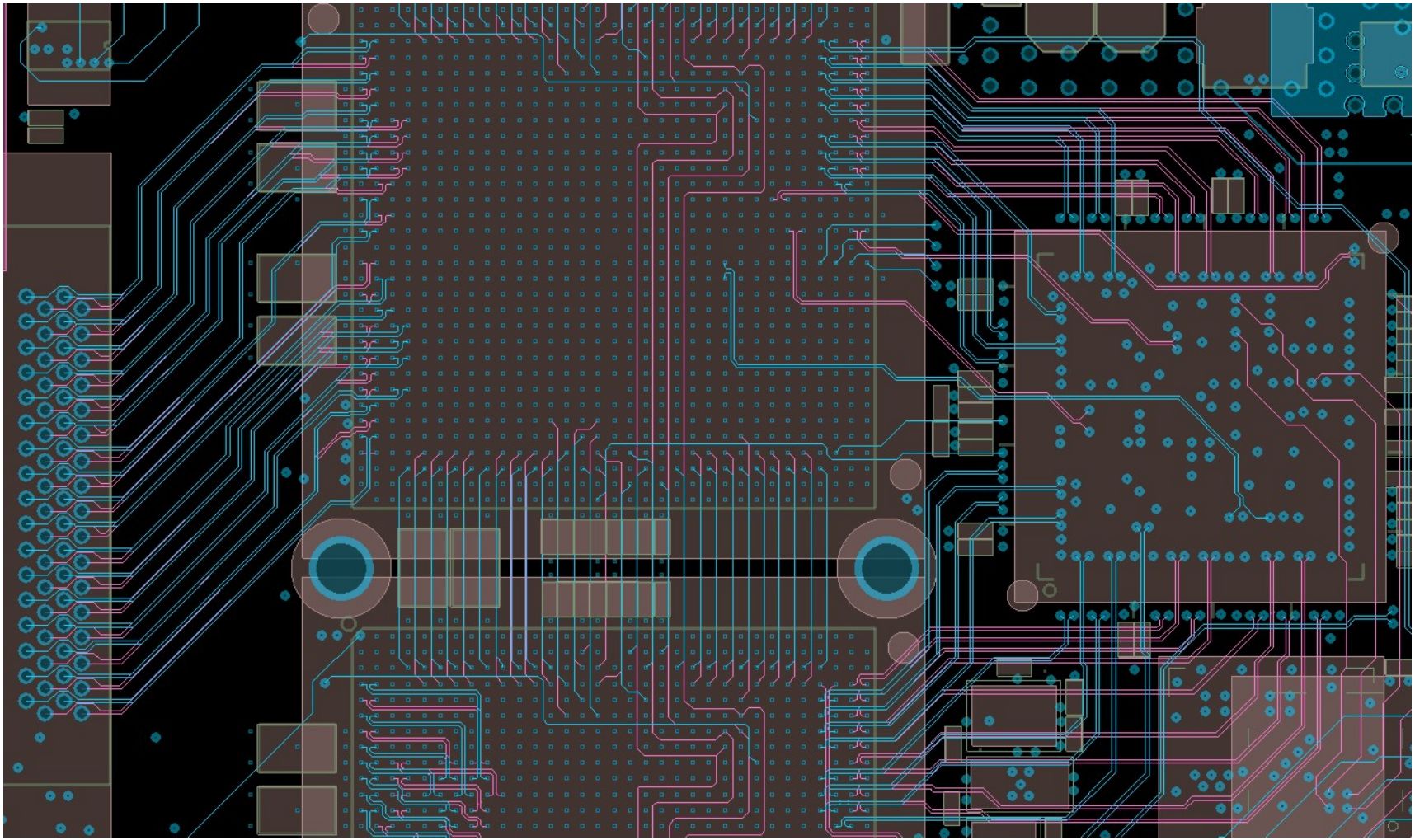
Example 2; 12GHz ADC





1 x 12GHz sampler board =
8 x 500MHz downconverters + 4 x dual-1GHz sampler boards

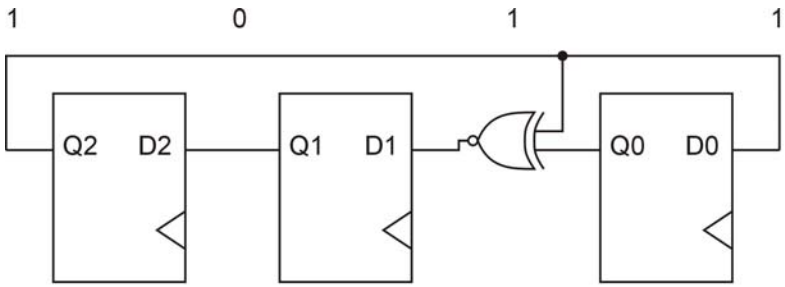
Example 3; LVDS routing



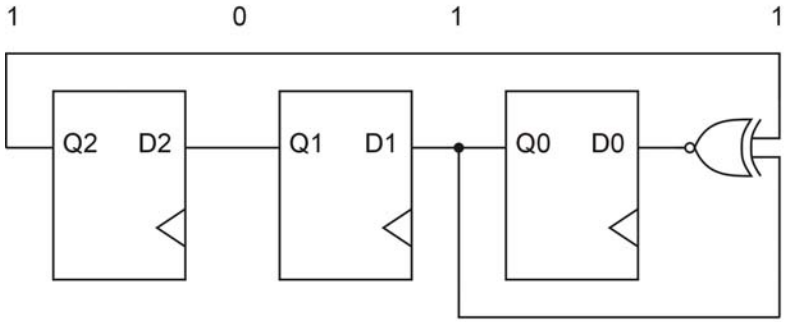
FPGA Signal Processing

- Numerically controlled oscillator (NCO);
  - digital downconversion
  - phase-offset (lobe rotation) compensation
- FIR filters;
  - Sub-nanosecond delay tracking
  - Bandwidth selection
- Whole nanosecond digital delay lines
  - FPGA RAM, and logic cell multiplexers
- Cross-correlation (lag domain)

Linear Feedback Shift Register (LFSR)



Q[2:0] Sequence
000b = 0
010b = 2
110b = 6
101b = 5
011b = 3
100b = 4
001b = 1



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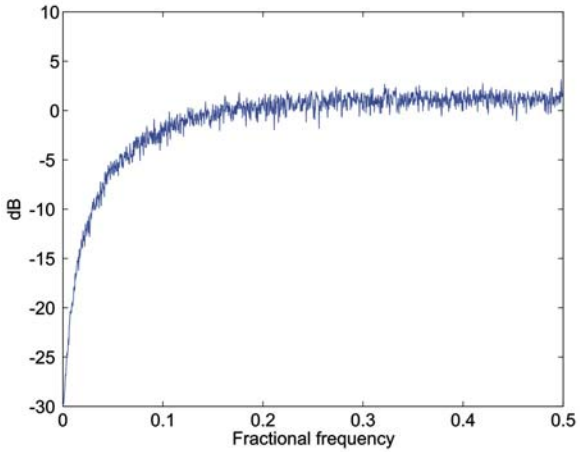
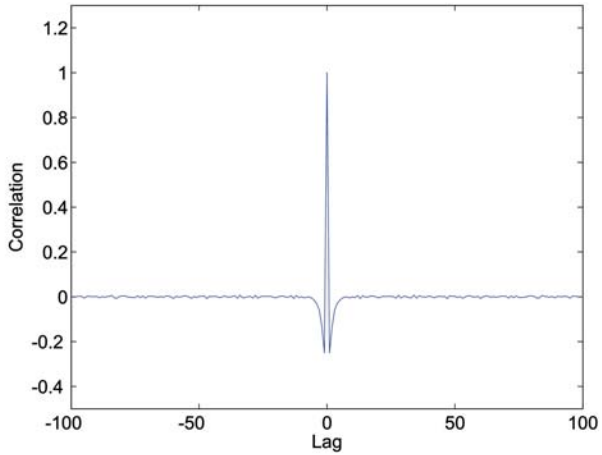
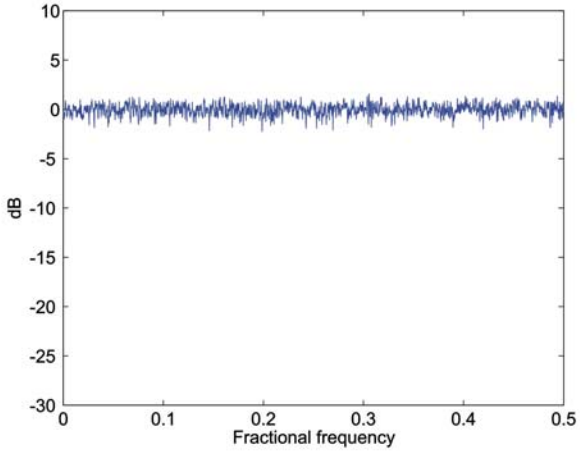
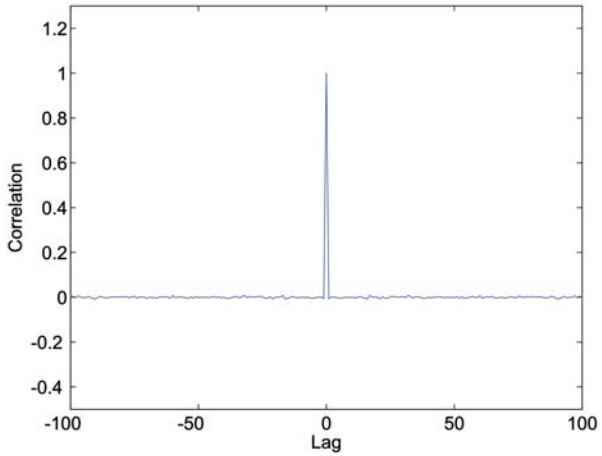
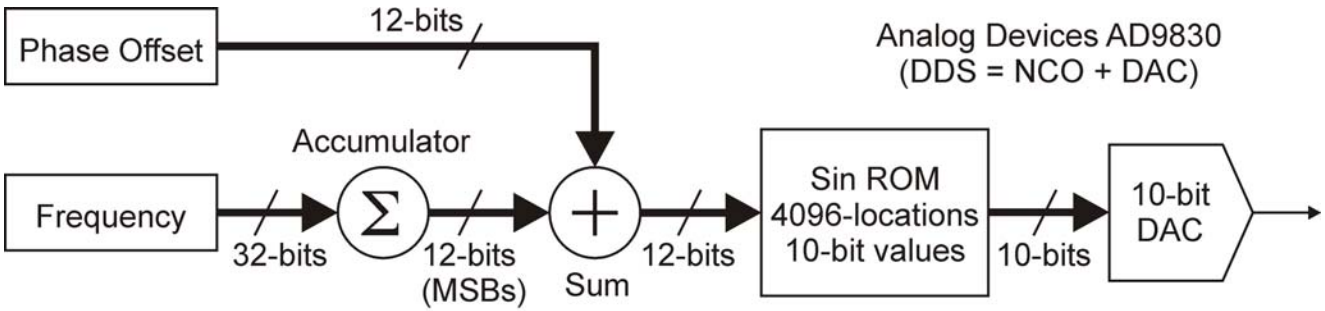


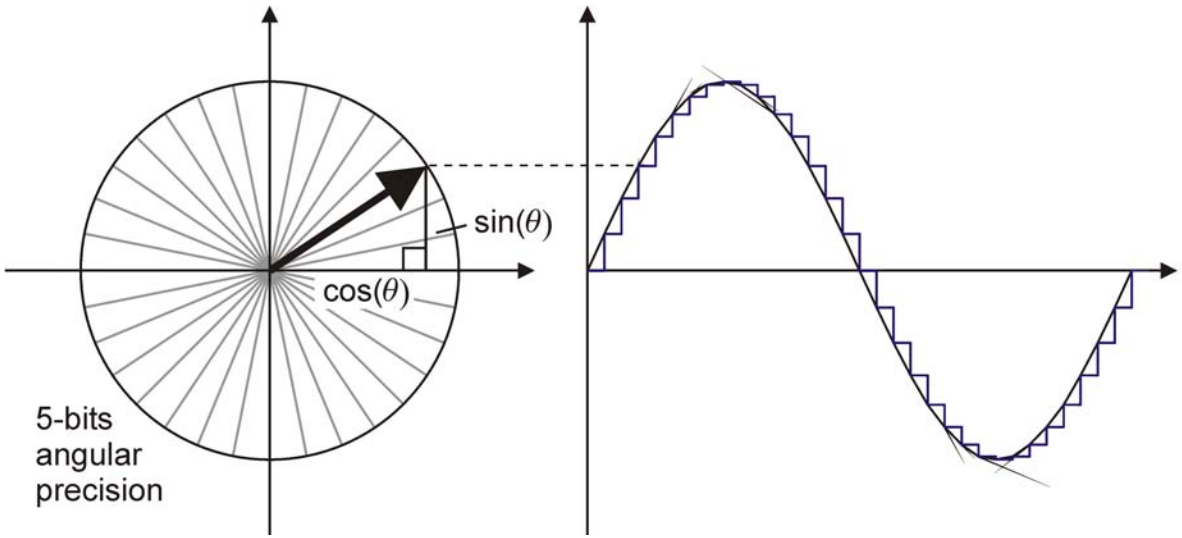




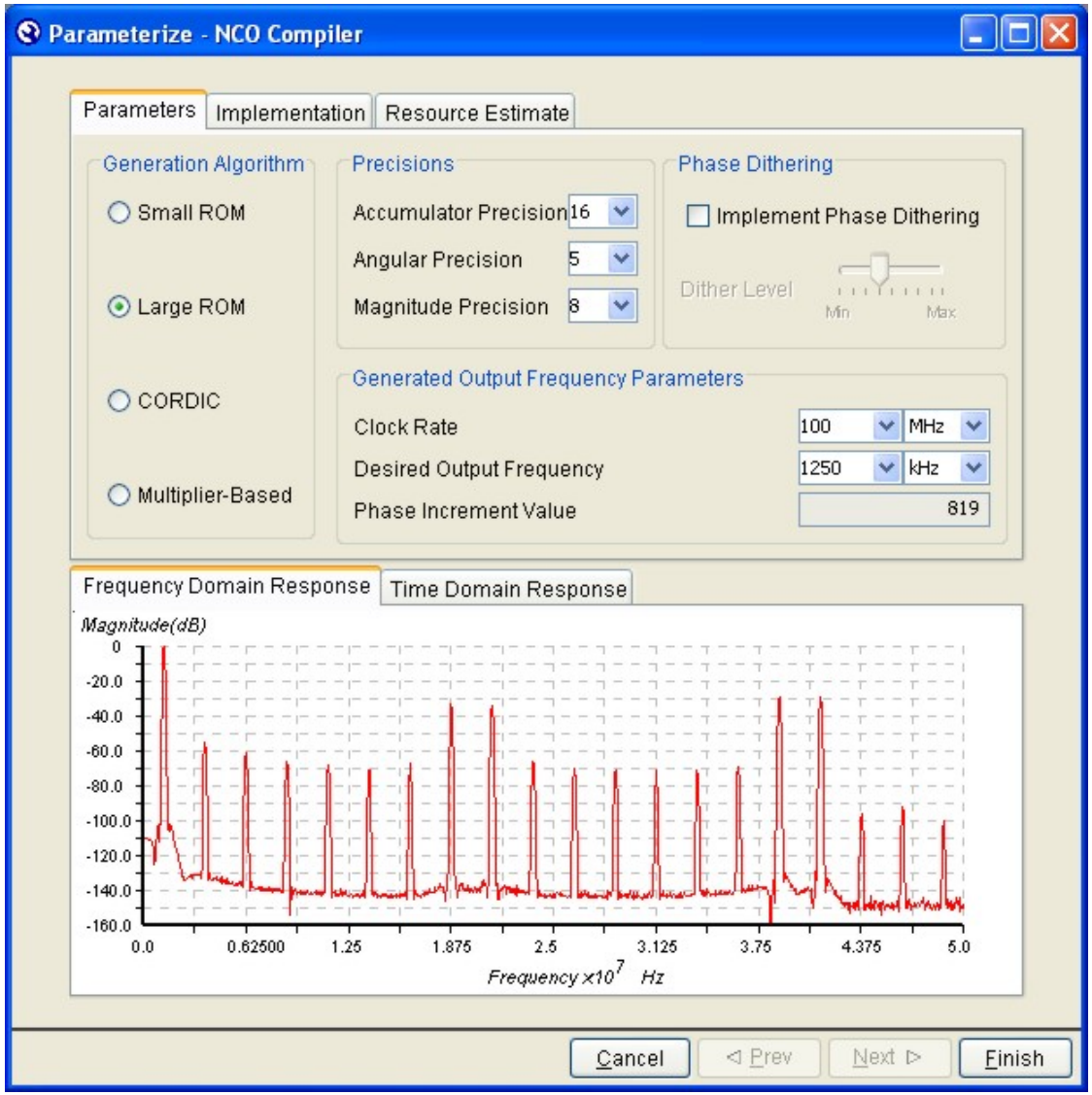


Numerically controlled oscillator (NCO)

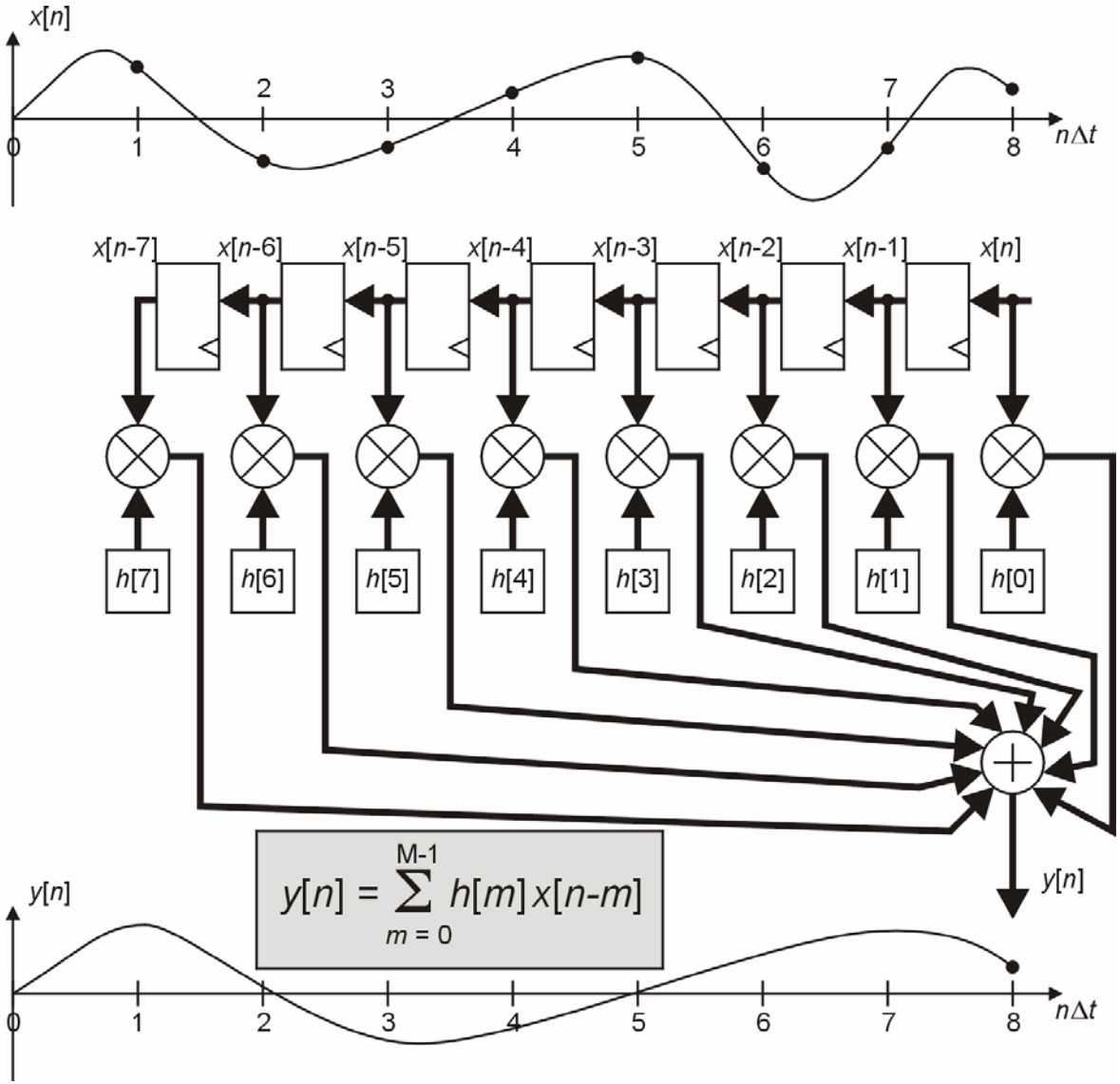




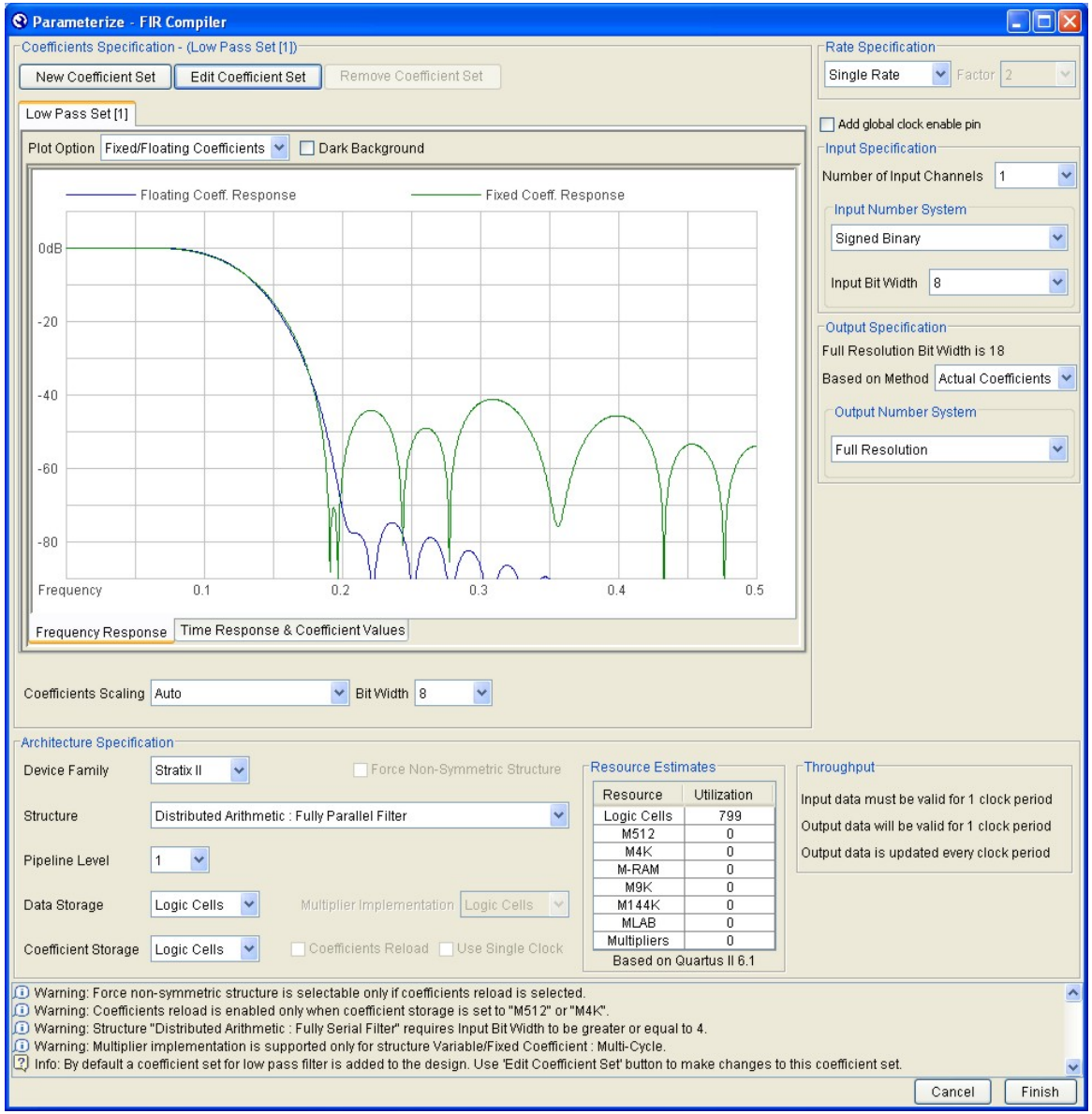
Altera NCO Compiler



FIR Filtering



Altera FIR Compiler



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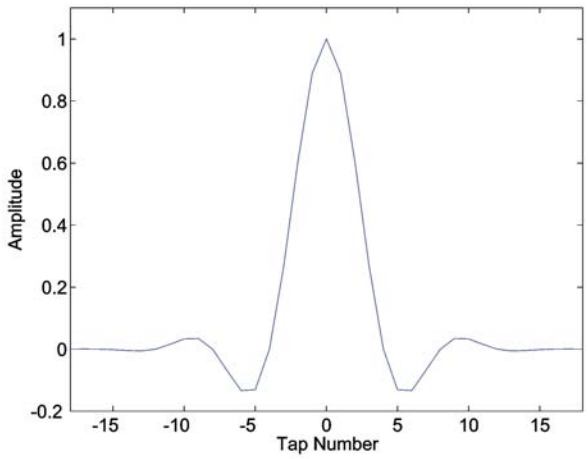

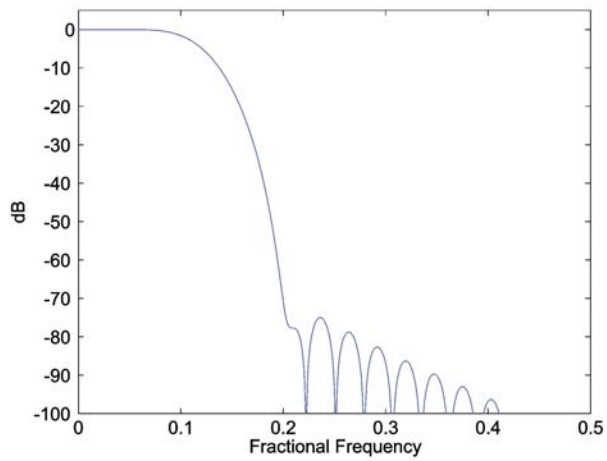

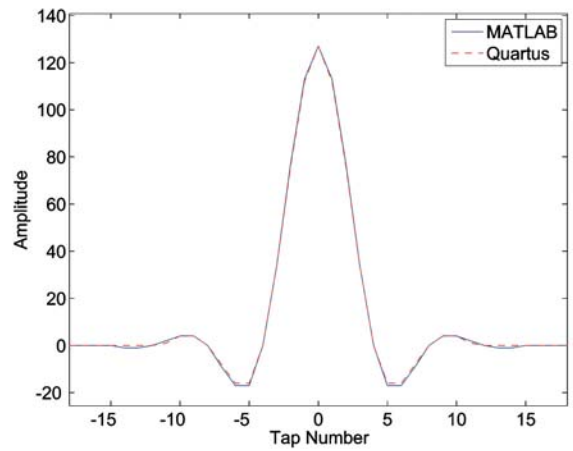

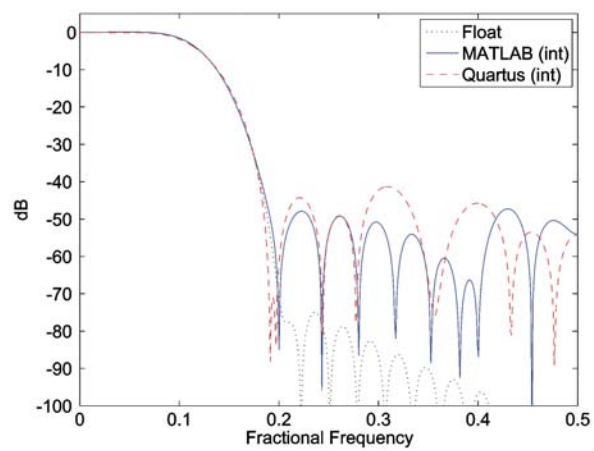

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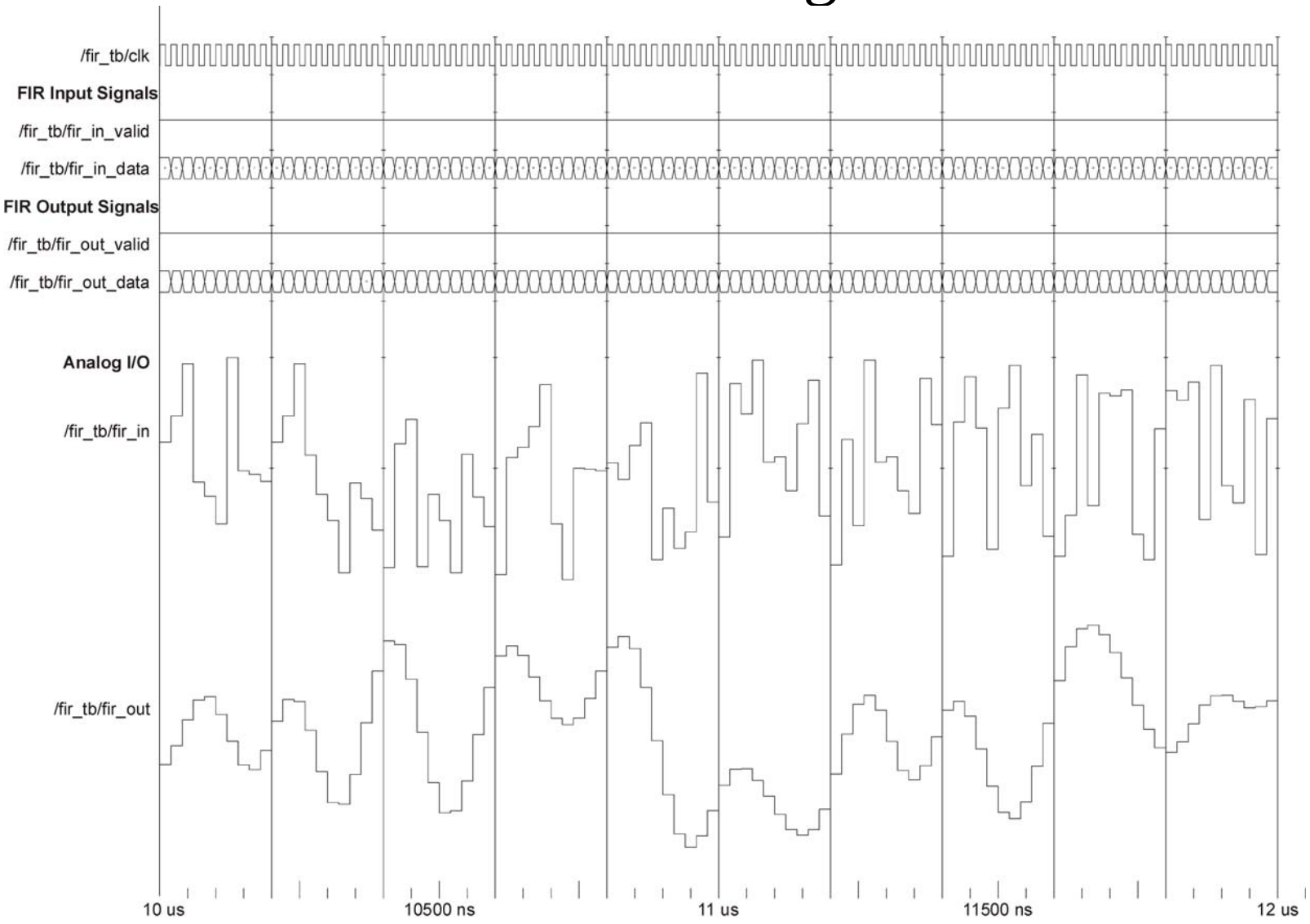

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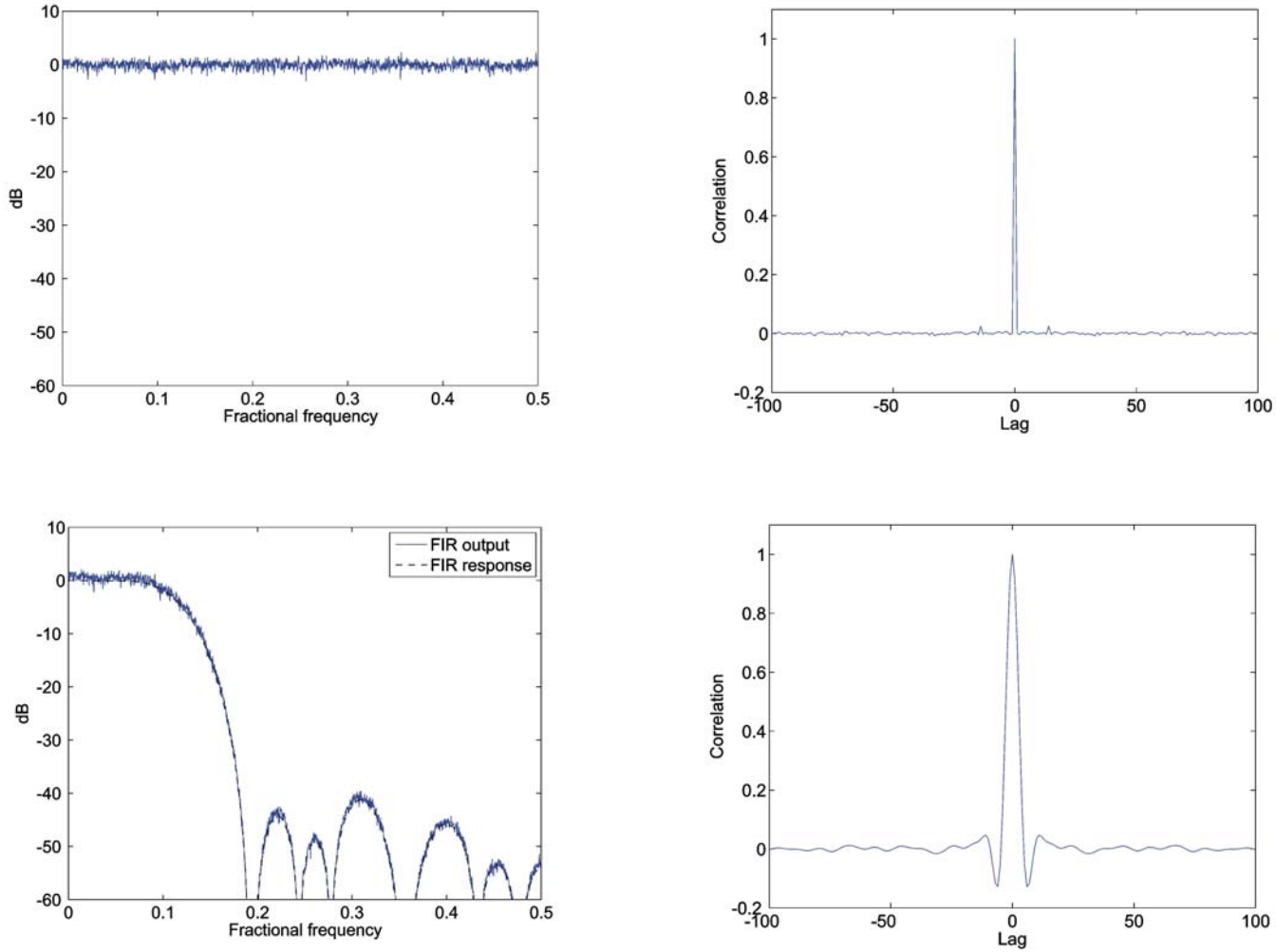
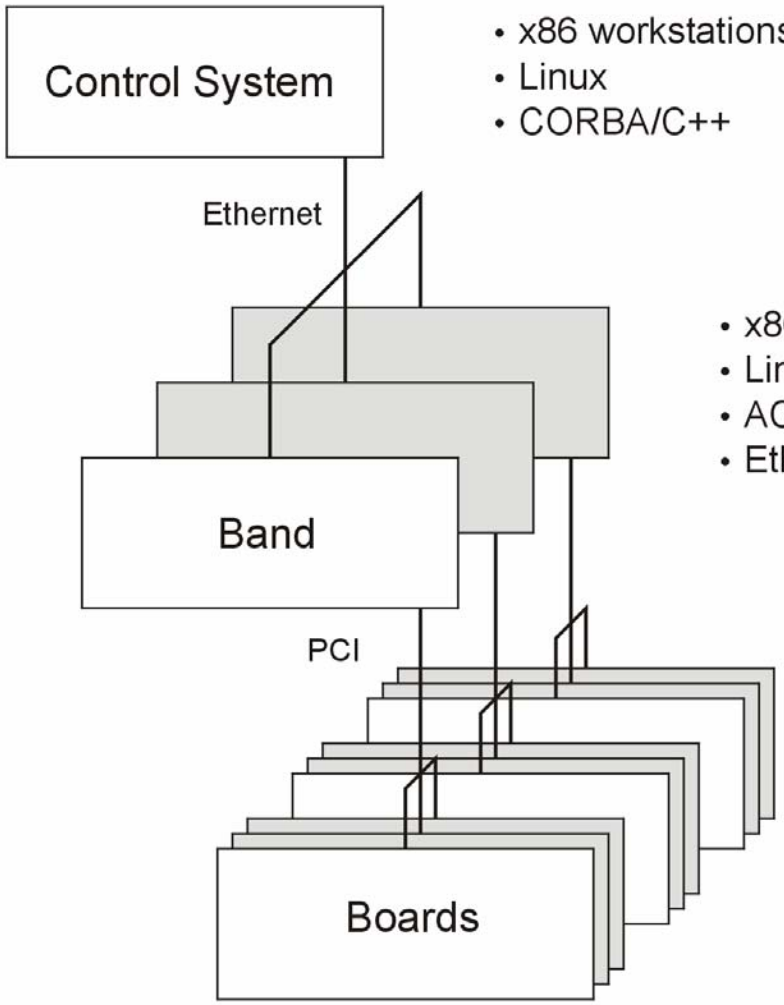


Control software



- x86 workstations
- Linux
- CORBA/C++

- x86 cPCI boards
- Linux
- ACE/C++
- Ethernet-over-PCI driver

- PowerPC cPCI boards
- Linux
- ACE/C++
- Ethernet-over-PCI driver
- FPGA interface driver
- Sensor drivers