3D Integration Using Wafer-Level Packaging

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Agenda

- Wafer-Level Packaging Technology Overview
- IRAD development on large arrays
- Advanced Integration
- Next Level Assembly
- Summary / Future work
What is Wafer-Level-Packaging?

- Add inter-cavity interconnects and cavity ring
- Stack and bond multiple wafers, then dice
- Forms a hermetically packaged 3-D integrated circuit
- Enables integration of different MMIC technologies

WLP provides low cost, high volume, hermetic packaging
Integrated Microwave Assembly Packaging
Wafer-Level Integration Benefits

- Hermetic
- Ultra-light weight, ultra-compact
- Low cost, high volume
- Performance enhancement

**Wafer-Level Integrated Package**

- Weight: < 50 mg
- Size: mm x mm x mm
- Assembly: mass parallel, wafer scale

**IMAs**

- Weight: g to >1000g
- Size: cm x cm x cm
- Assembly: serial, manual

Package near a thumb tack
Superiority And Affordability

- **Superiority**
  - Hermetic packaging in compact form factor
    - Protect MMICs against harsh environment
    - Enhance circuit reliability
  - Superb circuit performance
    - Good circuit isolation
    - Low transition loss
    - Low parasitics: eliminate wire bonds
  - High functional density
    - One package replaces many MMICs
    - Ultra compact, ultra light weight
    - Relax system requirement: decrease # of modules required, simple drive scheme

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<th>Integrated Microwave Assembly (IMA)</th>
<th>Wafer-Level-Package (WLP)</th>
<th>Factors of Improvement</th>
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- **Affordability**
  - Batch fabrication processes, low cost, high volume
  - Reduce higher order assembly cost, relax module assembly requirement

*Heterogeneous Integration Offers Superiority in Performance and Affordability in Cost*
2-Layer WLP

- Wafers are individually processed prior to bonding
  - No changes to standard MMIC processes
- ICIC = Intra-Cavity InterConnections
- BICIC = Backside ICIC

2-layer Bonding Process Flow

2-Layer WLP is Constructed by Bonding 2 Individually Processed Wafers
Integration Using Wafer-Level Packaging

- WLP is assembled using a low temperature wafer bonding process
- WLP technology is fully compatible with NGST MMIC production processes

Low temperature wafer bonding process is key to MMIC compatible, robust WLP
Examples of Packaged MMICs

Ku Band PA, WLP GaAs HEMT circuit

Ku Band LNA, WLP GaAs HEMT circuit

Q-Band LNA, WLP GaAs HEMT Circuit

W-Band PA, WLP GaAs HEMT circuit
Comparison of WLP and non-WLP circuits

ALH 140 vs. ALH140V3

- Conventional ALH140 (FIDR1/A-J103 1146A-031)
- ALH140V3 with WLP cover (WLP5/1/P200-001)

RF performance similar for WLP and non-WLP circuits
Converting Existing Chips to WLP

- Almost all existing chips can be converted into a WLP chip with a passive cover
- Layout changes are straightforward
- RF performance of converted chip will change depending on chip sensitivity, performance, and frequency
- Simulations may need to be performed to assess RF performance changes due to WLP cavity
- WLP conversion will generally increase the size of the chip
Heterogeneous Integration Example

- Integrated RF front end module with antenna
  - PA (GaAs HEMT)
  - 3 bit phase shifter (GaAs HEMT)
  - Interconnections (IC ICs)
  - Antenna
WLP Linear Array Demonstration

- Demonstrated fully functional front-end modules with a linear 4-element array
  - GaAs HEMT + passive
  - LNA + 3-bit PS + antenna in an integrated Q-Band WLP package
  - Successful integration to BFN board
  - Demonstrated electronic beam steering

**Integrated RF front-end modules w/ antenna**

**Measured Beam Pattern**

- \( \theta = 0^\circ \)
- \( \theta = 15^\circ \)

**Beam Forming Network (board)**

**WLP bottom side**

**WLP top side (antenna)**
WLP Demonstrations

- **WLP is fully compatible with NGST’s MMIC production processes**
- **Demonstrations to-date**
  - Different compound-semiconductor technologies w/ WLP
    - InP HEMTs
    - GaAs HEMTs
    - GaAs HBTs
    - GaAs Schottky diodes
    - InP HBTs
    - ABCS HEMT
    - MEMS switches
    - Passive components
  - Frequency bands w/ WLP
    - X-band
    - Ka-band
    - Q-band
    - Ku-band
    - V-band
    - W-band
  - Different circuit types w/ WLP
    - LNAs
    - PAs
    - Oscillators
    - Phase shifters
    - Shift registers
  - Substrate combinations w/ WLP
    - GaAs + GaAs
    - InP + GaAs
    - InP + InP
    - Quartz + Quartz
    - Si + InP
    - Glass + Glass
    - GaAs x 3
    - GaAs x 4
    - GaAs x 5
    - GaAs + Duroid
    - GaAs + InP + GaAs

**NGST has extensive experience in heterogeneous integration using WLP**
Package Integrity

- WLP packages passed the following tests:
  - Vibration-Sine
    - MIL-STD 883F, Method 2007.3, condition B
  - Mechanical Shock (Pyroshock)
    - MIL-STD 883F, Method 2002.4, condition B
  - Temperature Cycling
    - MIL-STD 883F, Method 1010.8, condition B
    - -55°C to 125°C, 50 cycles, MEMS
    - -55°C to 85°C, 300+ cycles, W-Band GaAs circuits
  - Hermeticity
    - MIL-STD 883F, Method 1014.11
    - He fine leak, condition A2, flexible
    - Radioisotope fine leak, condition B
    - Penetrate dye gross leak, condition D
  - Die Shear
    - MIL-STD 883F, method 2019.7
  - Environmental test: 85°C 85% humidity 7 days Ku band GaAs MMICs

WLP packages are hermetic, thermally and mechanically robust
Advanced Integration: Multiple Layer WLP

- 4-layer construction
  - Use bonded pair as starting units

Multiple Layer WSA Flow

Bonded Pair 1

Bonded Pair 2 or single wafer

Process Bonding layer if necessary (backside)

Wafer Bonding

ICIC (Front side)
BICIC (backside)
Bonding Layer

4-layer Bonding Process Flow

Bonded Pair 1

Bonded Pair 2

4-Layer Construction is Achieved By Bonding 2 bonded WLP pairs
X-Band Tri-Layer Tx/Rx Modules

Average mass: 12.9mg
Size: 2.5mm x 2mm x 0.46mm

- Next-Generation Large Aperture Array T/R Module
  - Ultra light weight (<15 mg)
  - Extremely compact (<5 mm²)

- Transceiver Module Performance Goal
  - FOM > 10,000
  - Reliability: MTTF > 10⁶ Hours

Demonstrated X-Band Integrated T/R Module
Microbump: Chip-Board Integration

- Developed microbump technologies for WLP-to-board attachment and integration

Microbumps on backside of the package

Sn/Pb microbump array

Cu stud microbump

Microbumps Enable WLP-to-Board Integration
Direct Board Attach Using Microbumps

X-ray result showing good board to chip interface

Good Chip-to-Board Microbump Interface
Epoxy Attach and Ribbon Bonds

Ku Band subarray board with WLP chips

Integrated Subarray Antenna Board

WLP modules

5 WLP MMIC fixture for environmental testing

WLPs are compatible with epoxy attachment

Normalized Amplitude

Azimuth (θ)

Normalized Amplitude

Azimuth (θ)
Summary & Future Work

• Demonstrated 100% MMIC compatibility of WLP technology with MMIC production processes
  – Many circuits using different semiconductor technology
• Demonstrated heterogeneous integration using WLP
• Demonstrated robust hermetic WLP packages
• Proven manufacturability (yield and performance)
• Long-term package reliability in progress
• Continue to develop/mature advanced integration technology
• Technology qualification in progress