PureB silicon photodiode detectors for DUV/ VUV/ EUV light and low-energy electrons

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[Logos of various institutions]
Outline

• Introduction
• Pure boron CVD technology
• Doping from pure boron layers
• Electrical properties of PureB p+n diodes
• Application as photodetectors for low-penetration-depth radiation and charged particles :
  • VUV, DUV, EUV
  • low-energy electrons
• Conclusions
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Pure boron CVD technology

700°C deposition

Not visible on the HRTEM:
- a few nm B-doping of the Si substrate below the $B_xSi_y$

Pure boron deposition from $B_2H_6$ gas in an AMSI Epsilon One Si/ SiGe epitaxial CVD reactor

- $\alpha$-Si
- $\alpha$-B $\sim$ 4 nm
- $B_xSi_y$ $\sim$ 1 nm
- Crystalline Si substrate
Constant boron deposition rate

Pressure: 760 Torr
Temperature: 700 °C
$\text{B}_2\text{H}_6$ concentration: 2%
$\text{B}_2\text{H}_6$ flow rate: 490 sccm
Other boron deposition properties

**Under the right conditions:**
- high selectivity to native-oxide-free Si surfaces
- uniform depositions for temperatures: 500 °C – 700 °C
- isotropic deposition on Si

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**Uniform coverage**

**Isotropic deposition**
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Doping from pure boron layers
Doping from pure boron layers

5 s exposure: \(\sim 1\) monolayer = \(6.78 \times 10^{14}\) cm\(^{-2}\)

10 min exposure: \(\sim 10^{17}\) cm\(^{-2}\)
After B-layer removal: $\sim 10^{14}$ cm$^{-2}$ boron concentration left
This exceeds the solid solubility $\Rightarrow$ some $B_xSi_y$
Sheet resistance measurements

B-layer resistivity very high: $10^4$ ohm-cm (semi-metal)

Doping of Si dominates sheet resistance
Post-processing for reduction of series resistance

in-situ thermal annealing and/or selective epitaxial Si/ SiGe growth:

![Graph showing the reduction of series resistance with post-processing techniques. The x-axis represents post-processing time and temperature, while the y-axis represents series resistance. The graph includes points for as-deposited material, 5 min at 800 °C, 1 min at 850 °C, 30 nm selective epitaxial Si growth, and Ø 3.7 mm.](image-url)
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Enhanced diffusion effects

No real evidence of transient or boron enhanced diffusion has been found.

Epitaxially-grown boron marker before and after PureB-deposition:

difference within experimental uncertainty
Electrical test structures

(1) $p^+n$ diodes
n-doping $\sim 10^{17}$ cm$^{-3}$

(2) $pnp$ bipolar transistors
emitter = B-layer

B-layer deposited in contact window, metallized immediately with Al/Si(1%)
$p^+n$ forward diode characteristics

Same behaviour at both temperatures:
- ideal characteristics
- saturation current decreases with deposition time
- series resistance first decreases and then increases

Behaves like conventional deep $p^+n$ junction!
p+n reverse diode characteristics

High electric field at perimeter lowers breakdown voltage
Use guard ring, but not seen for low substrate doping

n-doping
\( \sim 10^{17} \text{cm}^{-3} \)
pnp transistor characteristics

Base current level decreases with deposition time
1 min attractive:
- current gain comparable to conventional implanted-emitter pnp
- series resistance low
The B-layer suppresses the injection of electrons from the substrate $\Rightarrow$ B-layer thickness determines the current gain

Sarubbi, IEEE-TED 2010
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Lithography roadmap down to 10 nm features

EUV: supports 22 nm and 16 nm nodes with a single projection system
Challenging DUV/ VUV/ EUV detection

**VUV/ EUV**

High photon energy

**DUV**

Extremely small Penetration depth in Si

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Penetration depth in Si vs. incident radiation wavelength / photon energy.
Challenging DUV/ VUV/ EUV detection

Ideal spectral responsivity of Si-based photodetectors
Optical performance

EUV optical performance

Measured spectral responsivity of EUV PureB diodes with a 2.5 min B-deposition compared with a commercial $n^+p$ photodiode and the theoretically attainable values for an ideal Si-based photodetector.
Optical performance

**DUV/VUV optical performance**

Measured responsivity of PureB-diodes in DUV/VUV spectral range compared with other state-of-the-art photodetectors.
Performance stability

EUV responsivity degradation

Shape of the EUV spot (irradiance in the high power region is 3 W/cm² [24]) and the EUV-induced carbon contamination layer.

Ratio of measured EUV spectral responsivity after/before intense EUV irradiation (220 kJ/cm²), compared to the calculated ratio of responsivity based on the same diode with/without a 20 nm carbon layer.
Performance stability

**DUV/VUV responsivity degradation**

~ 4 nm silicon oxide layer was measured on the diode surface
Performance stability

DUV/VUV responsivity degradation

Oxide-free boron surface

High Stability
Robustness

H* cleaning

Filament enhanced H* cleaning setup

Plasma-generated H* cleaning setup

Micro-image of the EUV contaminated sample before / after 2 hours’ H* cleaning.

Measured responsivity before/after 4 hours’ H* cleaning
Crucial throughput requirement: 100 wafers per hour

EUV source: the most difficult challenge

MIRRORS NOT LENSES

2 wafer stages

3 types of detectors developed by DI MES

1. Energy sensor

2. TIS (transmission imaging sensor)

3. Spot/slit sensor
EUV Product Roadmap

2006
ADT
Resolution = 32 nm
NA = 0.25, σ = 0.5
Overlay < 7 nm
Throughput 5 WPH @ 5mJ/cm² ~8W

Main improvements
1) New EUV platform :NXE
2) Improved low flare optics
3) New high σ illuminator
4) New high power LPP source
5) Dual stages

2010
NXE:3100
Resolution = 27 nm
NA = 0.25, σ = 0.8
Overlay < 4.5 nm
Throughput 60 WPH @ 10mJ/cm² >100W

Main improvements
1) New high NA 6 mirror lens
2) New high efficiency illuminator
3) Off-Axis illumination option
4) Source power increase
5) Reduced footprint

2012
NXE:3300B
Resolution = 22 nm
NA = 0.32, σ = 0.2-0.9
Overlay < 3.5 nm
Throughput 125 WPH @ 15mJ/cm² >350W

Main improvements
1) Source power increase
2) Off-Axis illumination option
3) New high efficiency illuminator
4) New high NA 6 mirror lens

2013
NXE:3350C
Resolution = 16* nm
NA = 0.32, OAI
Overlay < 3 nm
Throughput 150 WPH @ 15mJ/cm² >550W

Platform enhancements
1) Source power increase
2) Off-Axis illumination option
3) New high efficiency illuminator
4) New high NA 6 mirror lens

* Requires <7nm resist diffusion length
Extremely complex

Detector elements: photodiodes, temperature sensors, absorber layer stacks, different filter layer stacks, 5 different types of alignment marks, two-sided contacting.

**Good manufacturability**
- IC processing compatibility
- flexibility
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Low-Energy Electron Detection

Challenges: low range in Si

\begin{itemize}
  \item 10 keV: \sim 1 \mu m
  \item 2 keV: \sim 200 nm
  \item 1 keV: (10 - 40) nm
  \item 500 eV: (5 - 15) nm
\end{itemize}

Metallization + coating layers + neutral p/n region < 10 nm

\textbf{DEAD LAYER LOSSES}

Device fabrication

1) **p⁺n junction formation**
- junction depth controlled with deposition time at 700 °C:
  - 2’ 40” for **1.8 nm** and 10’ for **5 nm** B-layer
- OPTIONAL Post-Processing: thermal annealing step for higher dopant activation / epitaxially grown 50-nm-thick B-doped Si layer

2) **Pure Al deposition**
- depositing Al with (1-2)% Si would leave Si precipitates when Al is selectively etched

3) **Anode contact definition**: diode area, contact ring on the perimeter of the diode, metal track, and contact pad
Device fabrication

Plasma etching
- Not selective to B-layer
- Promotes anisotropy
- Etching Al to about 100 nm thickness

Dilute HF etch stop
- Wet landing directly to the photosensitive surface
- **B-layer is highly resistant to diluted HF**
Relative Electron Signal Gain

State-of-art commercial detectors:
- vCD: low Voltage high Contrast Detector
- BSE: Backscattered-electron detector

\[ G_R (E_{beam}) = \frac{I_{ph} / I_{beam}}{(E_{beam} / e_0)(1 - \eta)} = \frac{G_{PH}}{G_{TH}} \]

\[ G_R = 0 \rightarrow I_{ph} = 0 \]

\[ G_R = 1 \rightarrow G_{PH} = G_{TH} \]
FEI electron detectors

Special requirements:
- very low capacitance
- low resistance
- many separated detector segments
- through-wafer holes

Solutions:
- low doped, high-quality, 40 µm thick epi-layers
- special metal grid processing
- through-wafer deep dry etching
Example of imaging capability (FEI ASB Magellan SEM)

SEM images of pollen taken with B-layer detectors

Sakic, IEDM 2010
Future processes
Selective Ge epitaxy on Si

- Unique feature: Large islands possible with sub-300nm transition at 700°C
- Uniform Ge surface compatible with CMOS planar processing
Ge-dots embedded in Si: defect-free

A μ-Raman strain measurement in the silicon above an embedded Ge quantum-dot [2].
Huandra, NanoLetters 2011
The first PureB application:

high-Q high-linearity varactor circuits made in silicon-on-glass technology
**SOG varactor diodes**

**True Two-sided contacting:** ideal 1-D behavior, eliminate parasitics

Diodes: low leakage, ultrashallow, made at low temperature

Nanver, IEEE JSSC 2011