Keck Institute for Space Studies
MMIC Array Receivers and Spectrographs Workshop
Pasadena, CA
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Digital Correlators for Spaceborne Earth Remote Sensing - Current Status and Near Term Technology Development

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1-d Fourier Synthesis Imager – X-Band Lightweight Rainfall Radiometer (LRR-X)

circa 1999-2004

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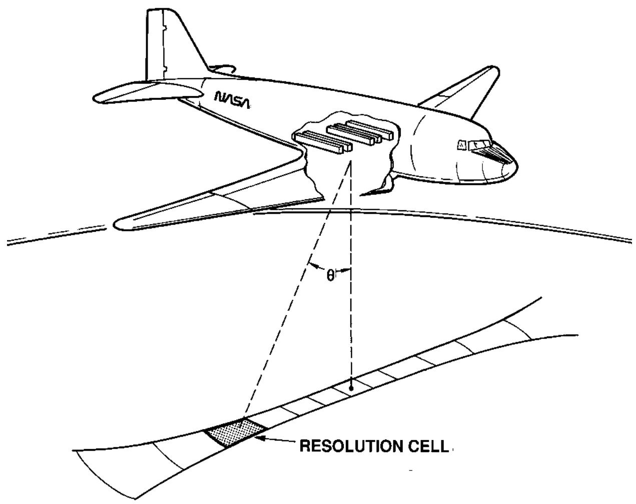
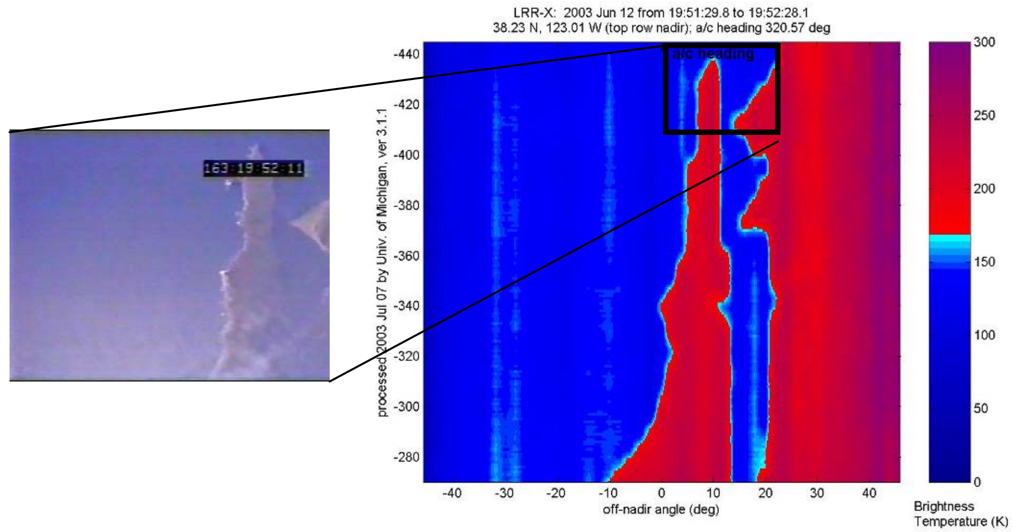
LRR-X





- Point Reyes National Seashore, CA
  - DC-8 nadir video camera (left)
  - LRR-X TB image at 10.7 GHz, H-Pol (right)
- LRR-X Specifications
  - Synthetic aperture 1 meter^2; Cross-track imaging
  - Spatial res @ 11 km altitude
    - 381 x 466 m (nadir); 1079 x 629 m (45^o cross track)
  - NEΔT of 0.3 K

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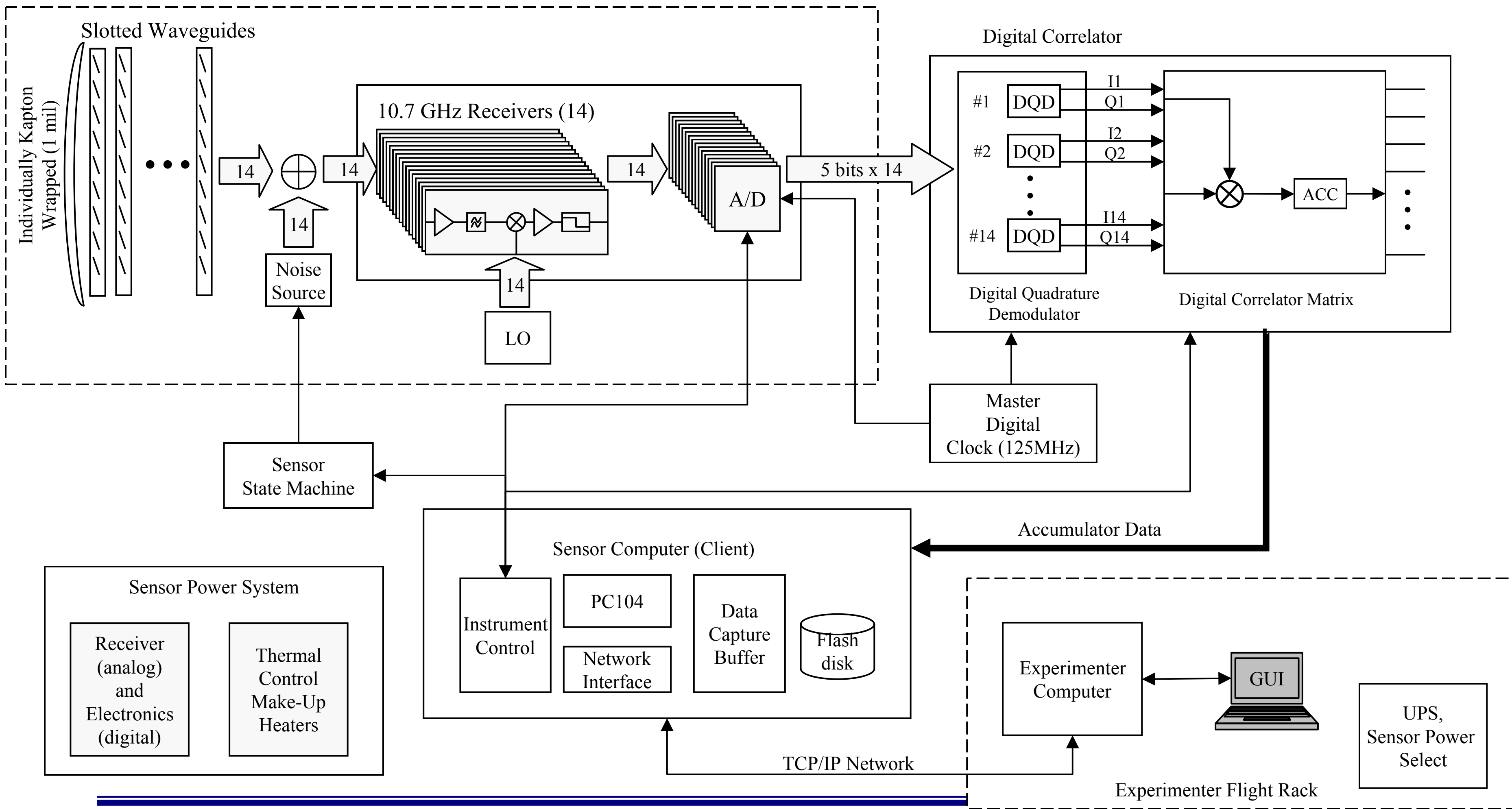
LRR-X Functional Block Diagram



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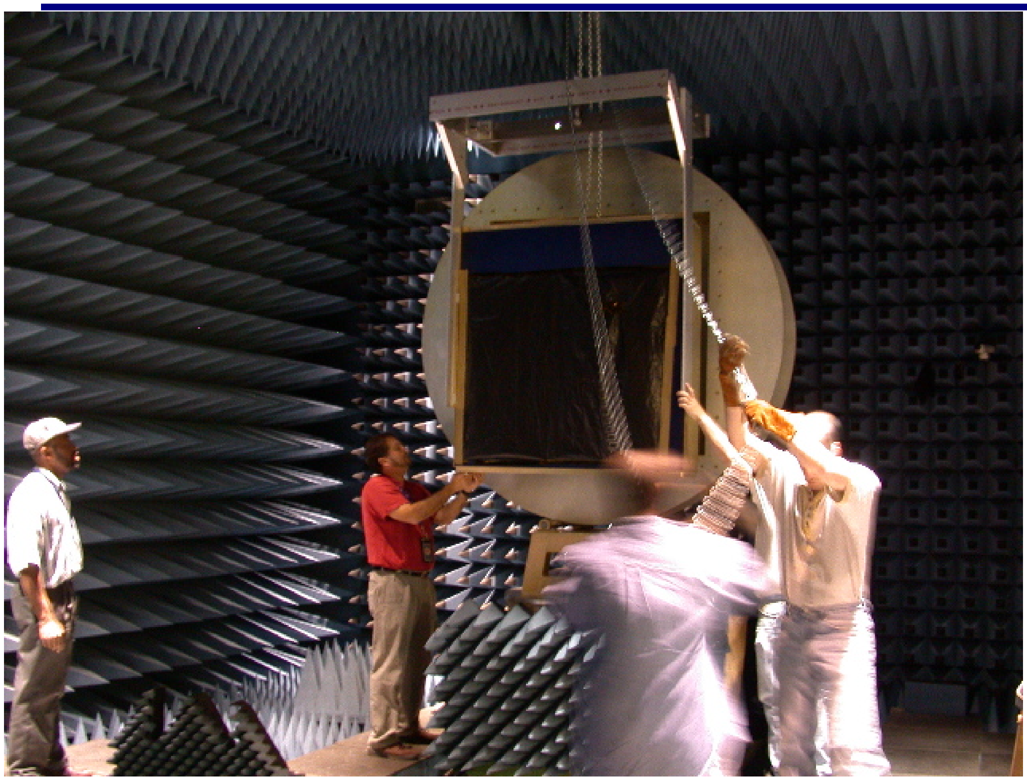
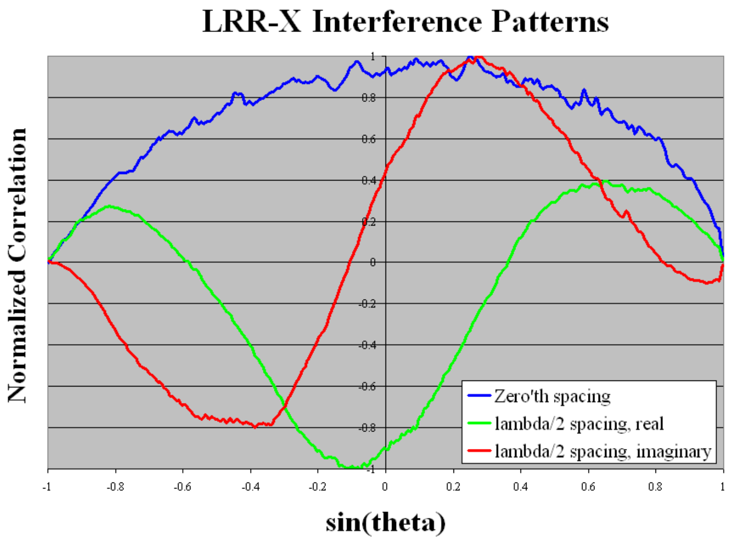
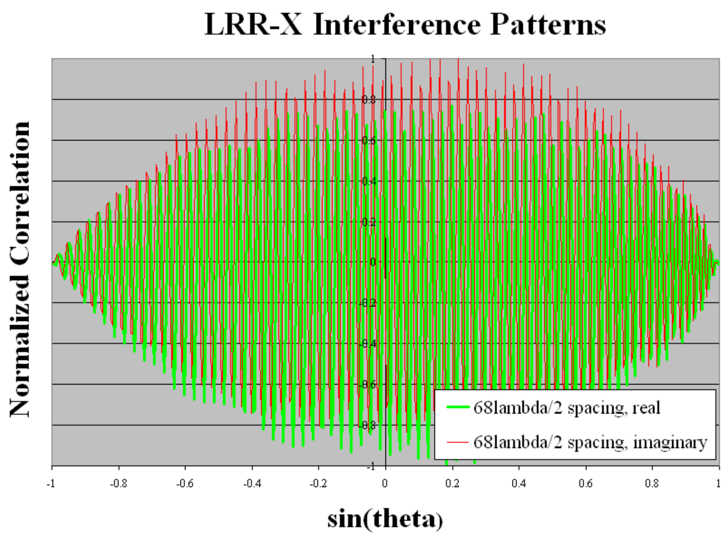
LRR-X Anechoic Chamber Cal Results
Spatial Interference Patterns







Antenna Array in Anechoic Chamber (above)
Zero'th spacing; λ/2 spacing, real & imaginary (top right)
68λ/2 spacing, real & imaginary (bottom right)

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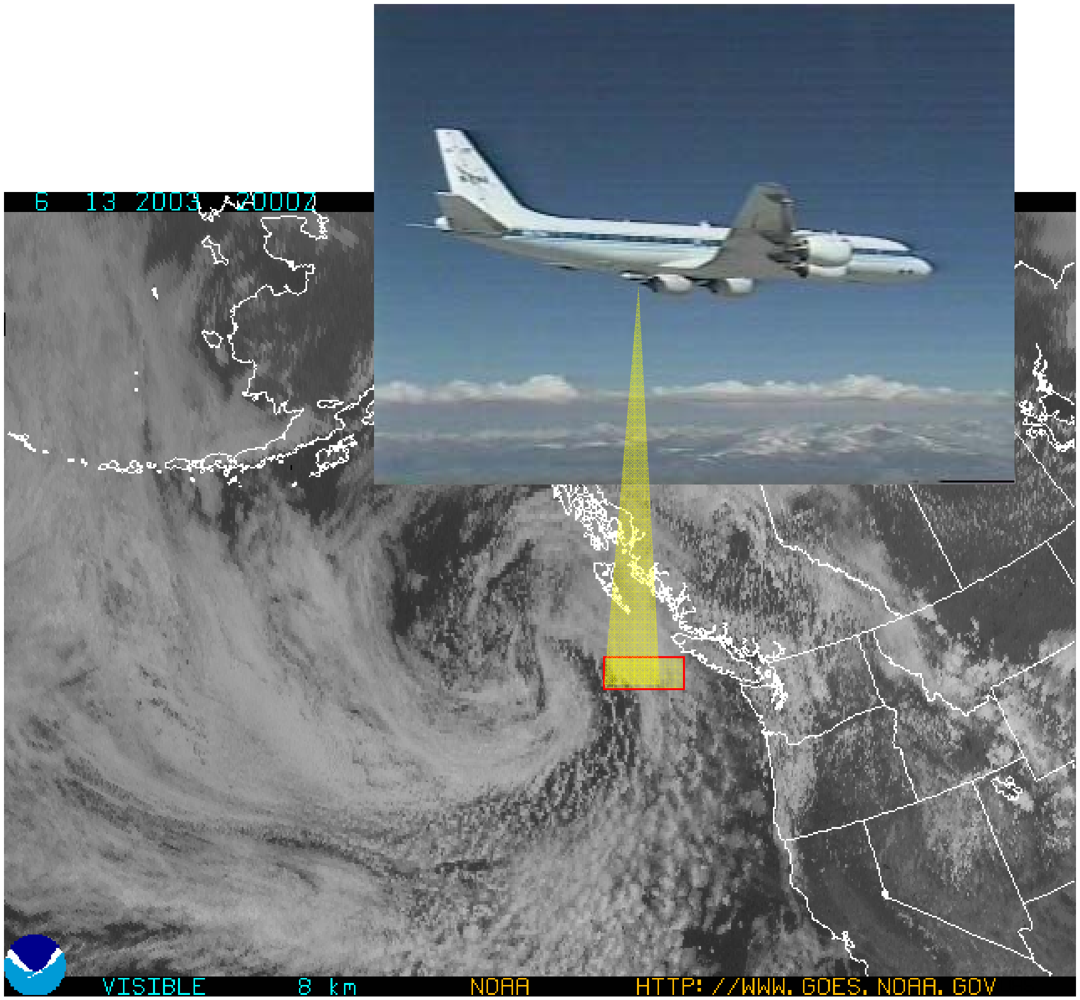
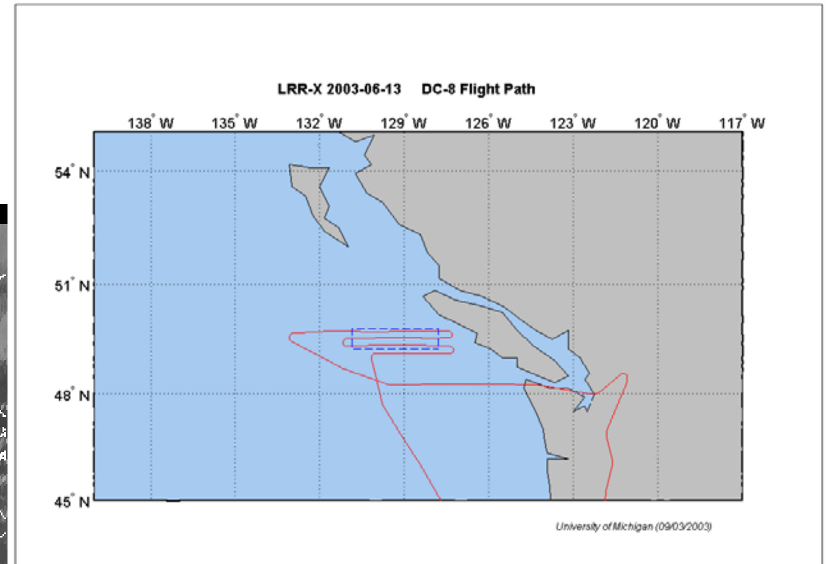
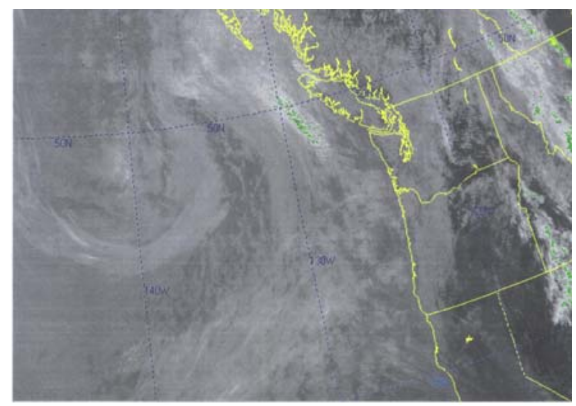
LRR-X 13 June 2003 Pacific Northwest Storm







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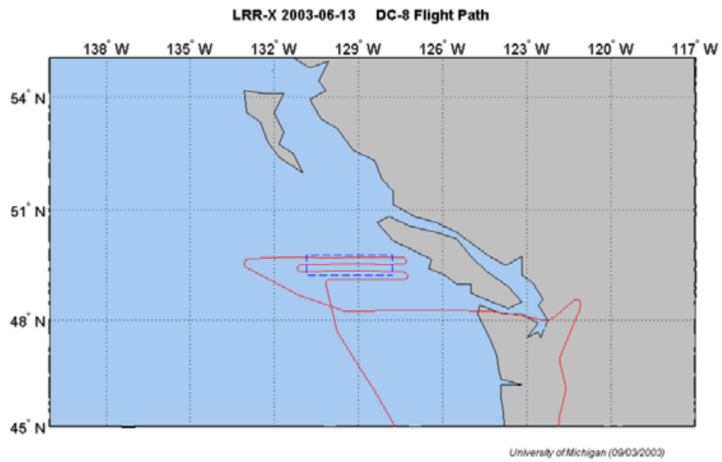
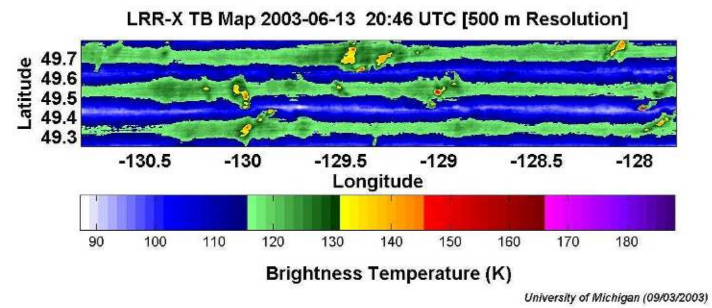
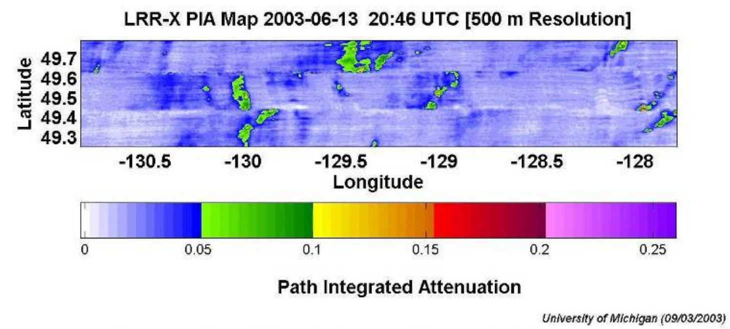
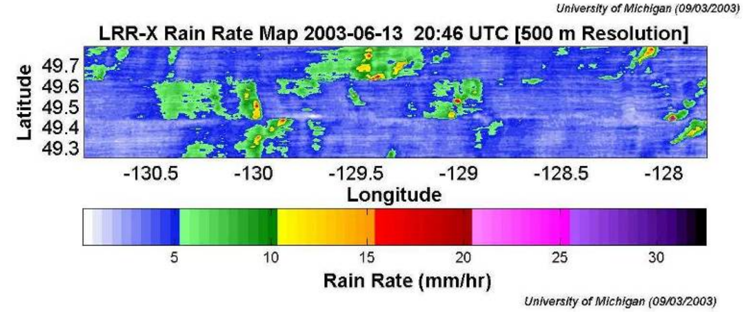
LRR-X Measured T_B and Retrieved Optical Depth and Rain Rate









- DC-8 Flight Lines on 13 June 2003 (above)
  - East/west raster scan over convective system west of Vancouver Island
- LRR-X raster scan images (right)
  - T_B (top) shows incidence angle dependence of ocean surface
  - Optical depth (middle) derived from T_B by inverting radiative transfer equation
  - Rain rate (bottom) derived from optical depth using Marshall-Palmer DSD and slab rain model

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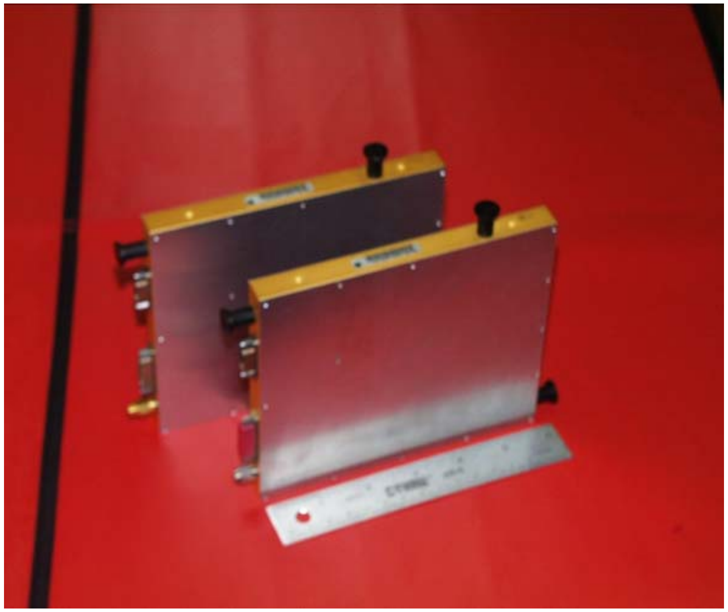
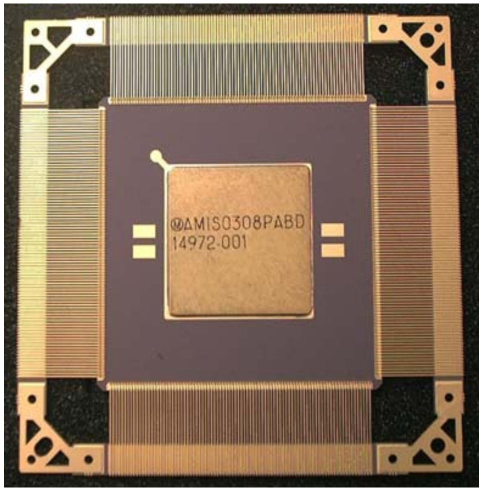
LRR Spaceflight Hardware Developments





Digital Correlation Radiometer
RF input from antenna / Digital output to correlator
DC Power = 550 mW; 0.55” thick
(TRW manufactured)

ASIC 25 channel complex correlator
Real time DSP @ 2960 GigaInstructions/sec
Input bandwidth: 11 Gigabytes/sec
DC Power required: 1500 mW
(U-Idaho/CAMBR manufactured)

Digital Correlator ASIC
(Developed for LRR Spaceflight Version)

- Design Requirements
  - Compute auto and cross correlations for the I and Q components of 25 input channels
  - Scalable beyond 25 channels
  - Process up to 224 megasample/second/channel
  - Integrate for up to 15 milliseconds
  - DC: 1.5W
  - Maximize radiation tolerance
- Ultra-Low Power (ULP) CMOS process
  - 0.5V internal logic with 3.3V output interface

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2-bit Analog-to-Digital Converter

(Developed for LRR Spaceflight Version)

- All three comparator thresholds independently controlled by 8-bit DACs
  - 100-250 mV (level 1), 220-280 mV (level 2), 250-400 mV (level 3)
  - 0.58 μV noise in DAC threshold levels
- Ultra-Low Power (0.5V logic) CMOS process

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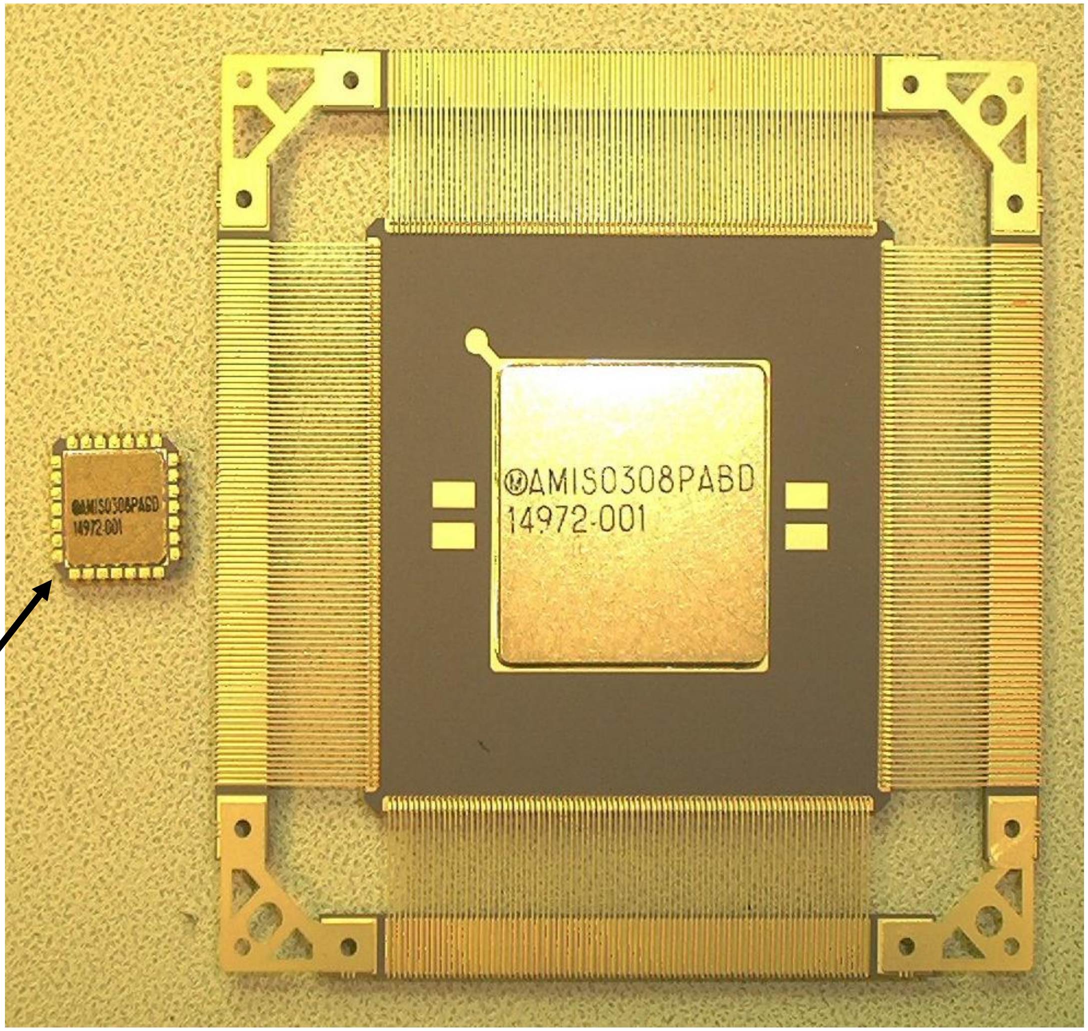
U-Idaho CAMBR ASICs
2-bit ADC and 25x25 Channel Correlator



ADC

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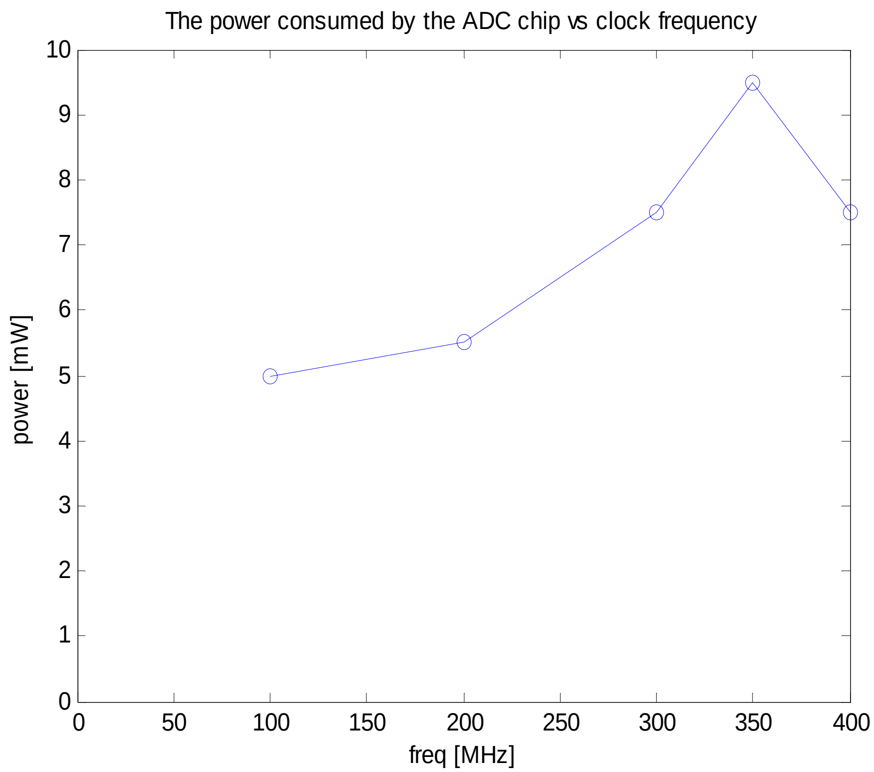
2-bit ADC Characterization Test – DC Power Requirement vs. Clock Speed

- Vary digitzation clock rate
- Monitor current drawn by all power supplies
- DC Power < 5 mW for f_c < 100 MHz
- Digitization quality still excellent at f_c = 300 MHz
- Some missed triggers beginning with f_c = 350 MHz



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2-d Fourier Synthesis Imager – Geosynchronous Earth Orbit Synthetic Thinned Aperture Radiometer (GEOSTAR)

circa 2003-present

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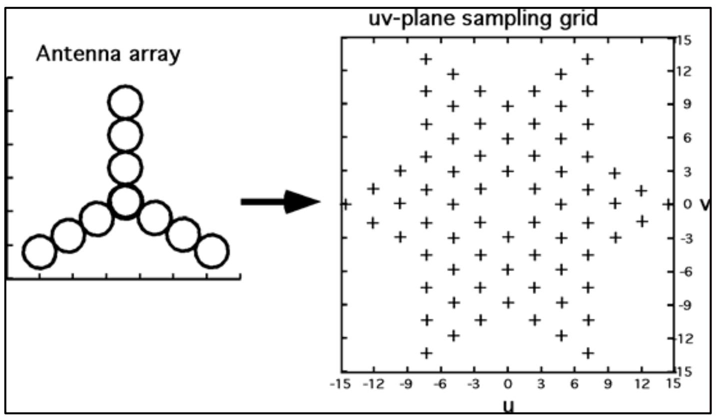
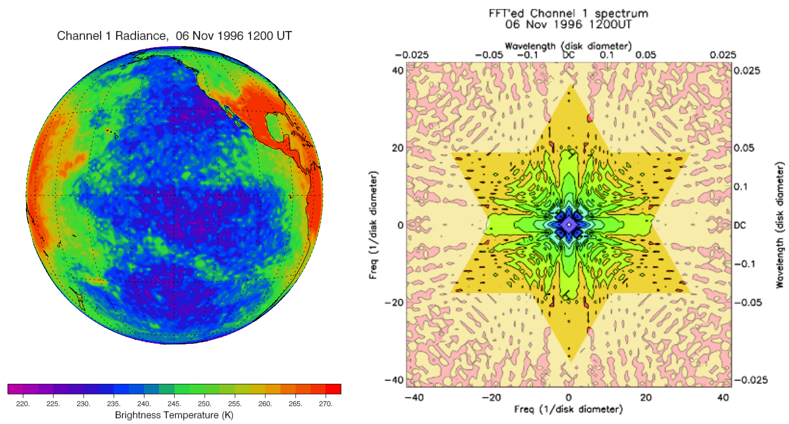
GEOSTAR – Microwave Temperature and Humidity sounder

- **Functionally equivalent to AMSU**
  - Tropospheric temperature sounding @ 50-55 GHz with ≤ 50 km resolution
  - Tropospheric water vapor sounding @ 183 ± 7 GHz with ≤ 25 km resolution
- **2-d Fourier Synthesis Imager to reduce mass & volume and eliminate moving parts**



Receiver array ➔ Resulting uv samples



Example: AMSU-A ch. 1

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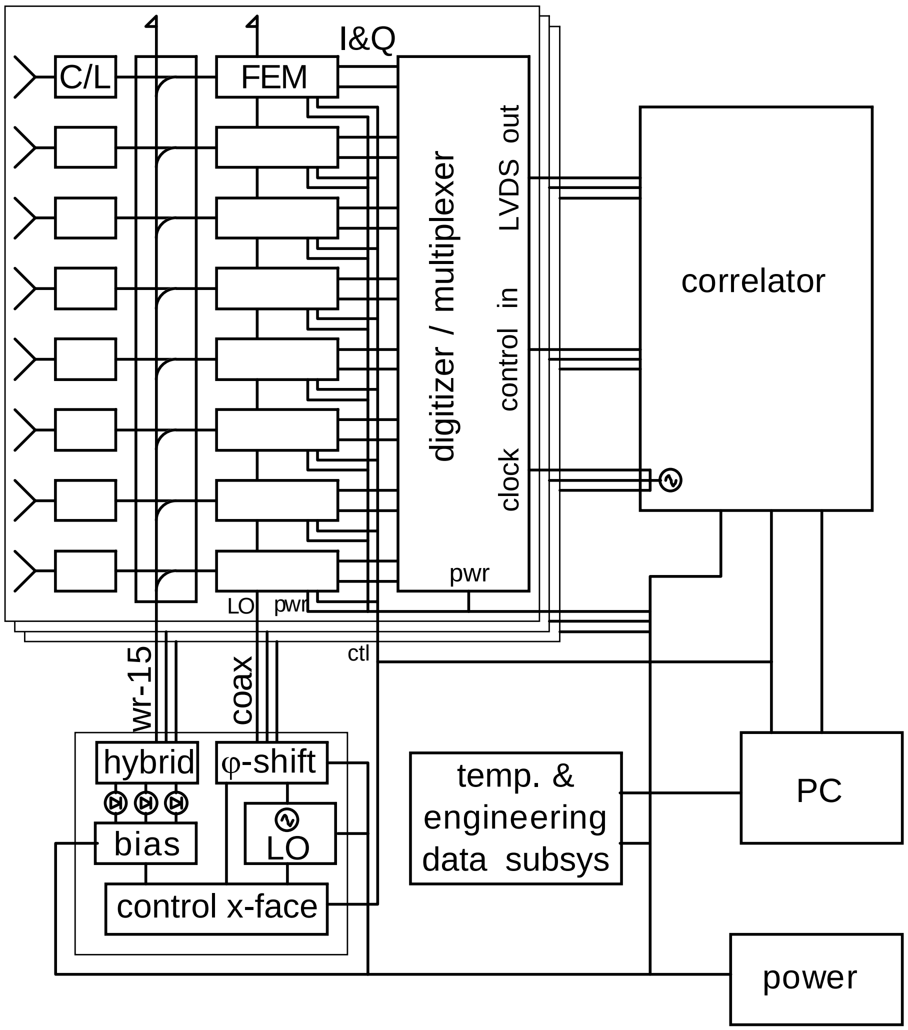
GEOSTAR Functional Block Diagram



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GEOSTAR Flight Correlator Design Study

- Correlator cell count = $3 * n^2 * m$
  - n = # of antennas/arm
    - n = 112 for 50 GHz array
    - n = 196 for 183 GHz array
  - m = # of multiplications/antenna pair
    - m = 4 for I*I, I*Q, Q*I, Q*Q correlations
- 50 GHz array: 150528 correlator cells
- 183 GHz array: 460992 correlator cells
- 200 MHz or 1000 MHz clock speed
- 1- or 2-bit ADC samples

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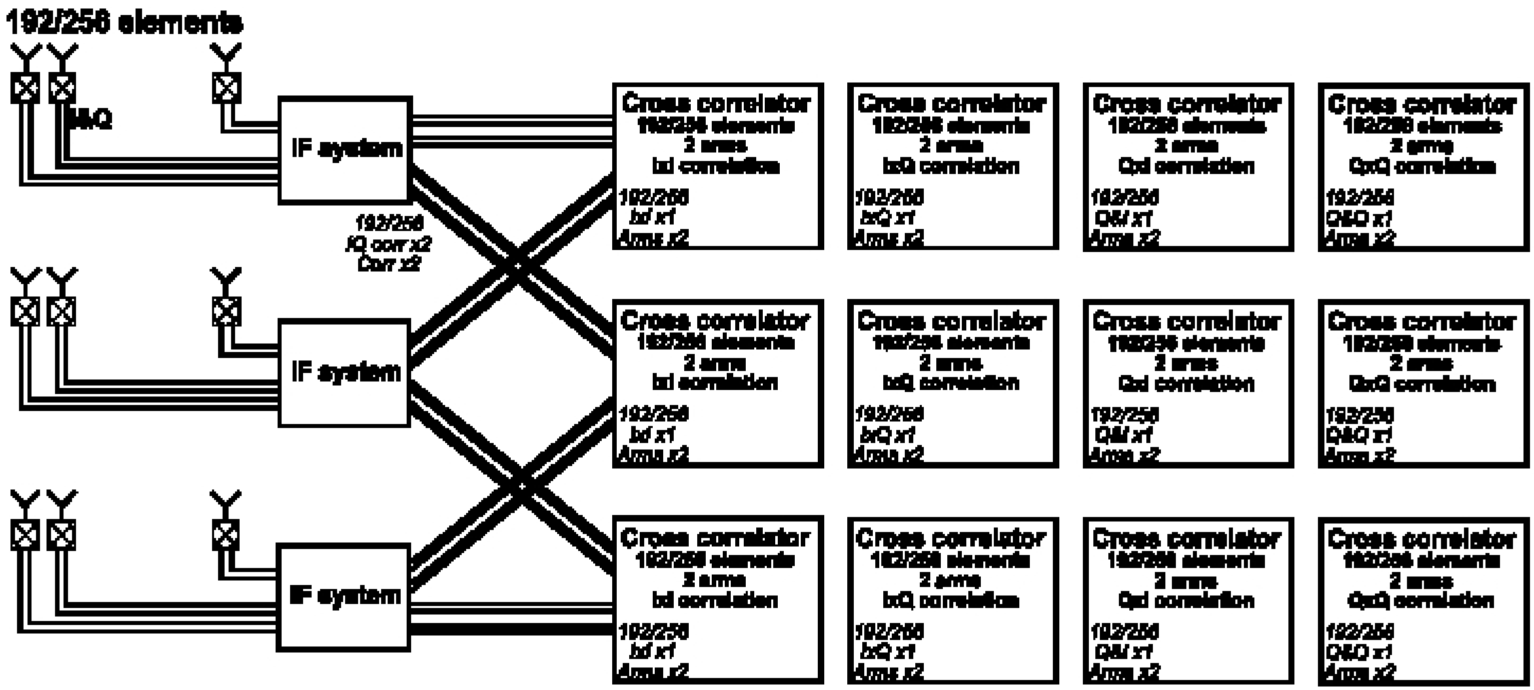
Design Architecture

- Power numbers presented here assume 183 GHz, 196 elements/arm 12-ASIC design
  - 12 identical ASICs (1 ASIC per arm pair per multiplication/accumulation type)
  - Additional assumption: point-to-point communications between digitizers and correlator ASICs (each ASIC input driven by a unique driver, not a “bus” with one driver and multiple receivers)



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Method

- Analyzed 250, 90 nm and 65 nm technologies
  - Detailed circuit level design of GeoSTAR specific correlator (multiplier-accumulator) cell @ 250 nm
  - Chip-level floorplanning of interconnect and clock distribution @ 250 nm
  - Parametric extrapolation of 250 nm power numbers to smaller technologies
    - Extrapolation method and accuracy has been verified by other project)

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Results

Bits / Ant.	Clock rate	Geom.	Power/ ASIC (W)
1	1 GHz	90 nm	3.8
1	1 GHz	65 nm	2.6
1	200 MHz	90 nm	1.1
1	200 MHz	65 nm	0.9
2*	1 GHz	90 nm	10.5
2*	1 GHz	65 nm	6.2
2*	200 MHz	90 nm	2.9
2*	200 MHz	65 nm	2.0

(*) 2-bit actual power consumption likely to be lower than this figure due to potential design optimizations not yet implemented

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Status and Plans

- 90 nm ULP available today, 65 nm ULP is on target for deployment in 1-2 year time frame
- Currently funded to build 50 channel version of ASIC correlator
  – Quad Flat Pack package to tackle internal ASIC design issues first, reduce risk
- Follow on steps (not currently funded)
  – Full 196 channel version with Ball Grid Array or Column Grid Array package
  – ULP 2-bit digitizer at ~1000 MHz

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