CASPER Collaboration for Digital Back Ends

Rapid Development of Instrumentation using general purpose FPGA boards, tools & libraries

(how to build 12 radio astronomy instruments in two years)

Dan Werthimer and Casper Group,
University of California, Berkeley

http://casper.berkeley.edu

CASPER

Center for Radio Astronomy Signal Processing and Electronics Research

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David MacMahon, Oren Milgrome, Mel Wright, Lynn Urry

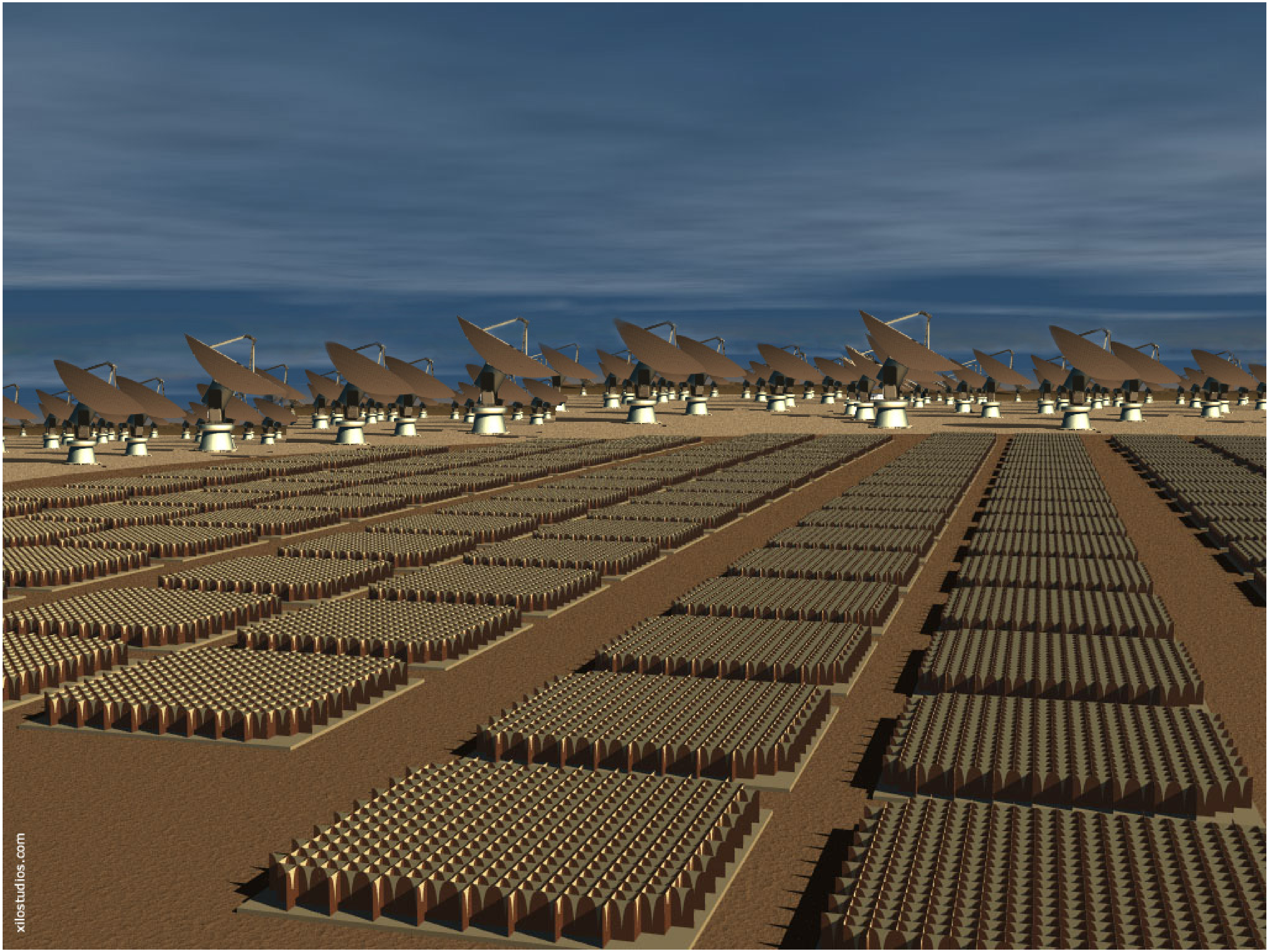
Berkeley Wireless Research Center:

Bob Broderson, Chen Chang, Kevin Chao, Pierre Droz,
Borivoje Nikolic, Brian Richards, , John Wawrzynek

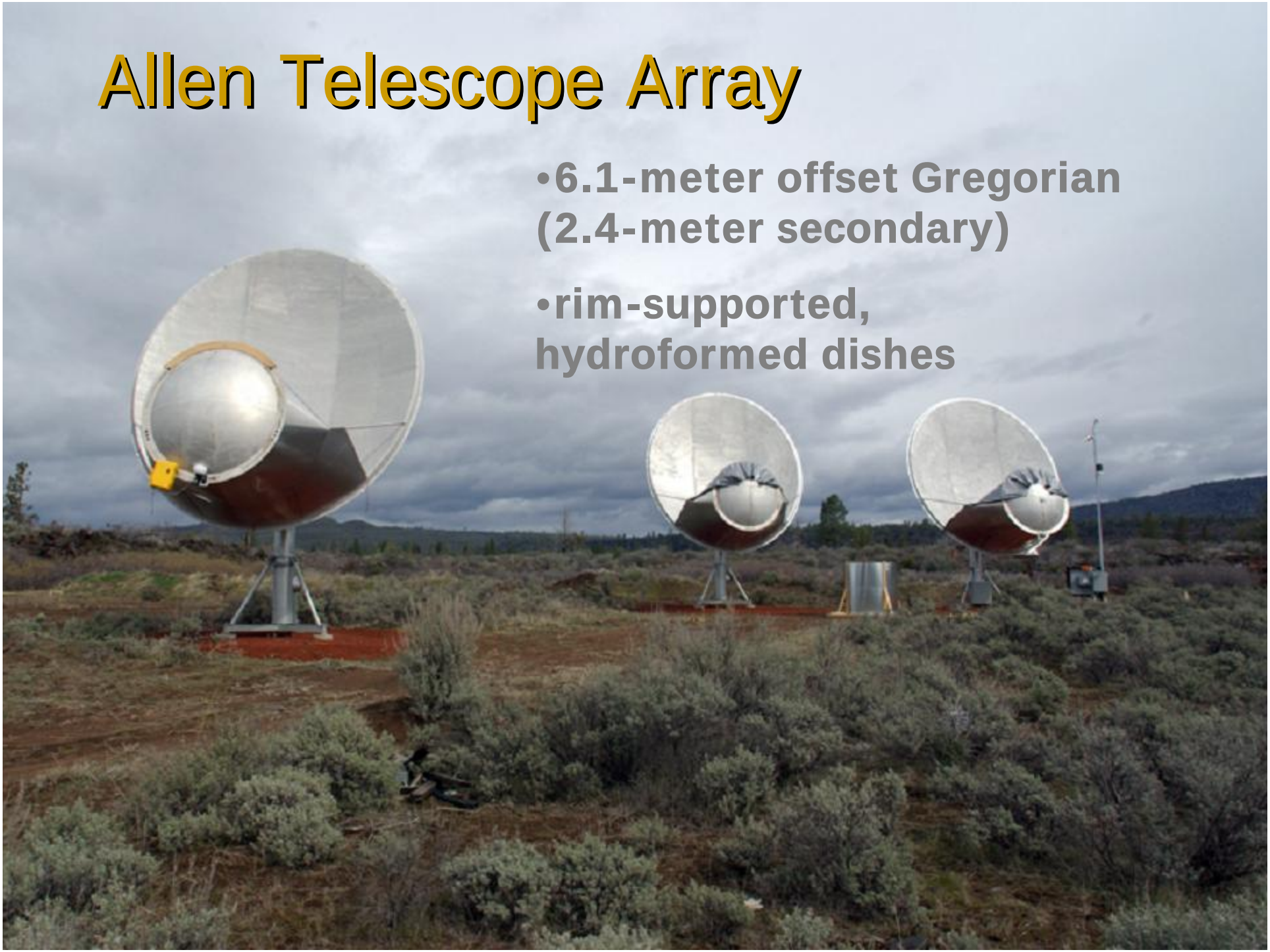
Collaborators:

Xilinx, Fujitsu, HP, Sun Microsystems, Agilent, NSF, NASA, NRAO, NAIC,
Chris Dick, Jeff Mock, CFA, Haystack, Caltech, Cornell, CSIRO/ATNF,
JPL/DSN, South Africa KAT, Manchester/Jodrell Bank, GMRT,
Bologna (SKA), Metsahovi Observatory/Helsinki University,
Chalmers (Sweden), Seti Institute

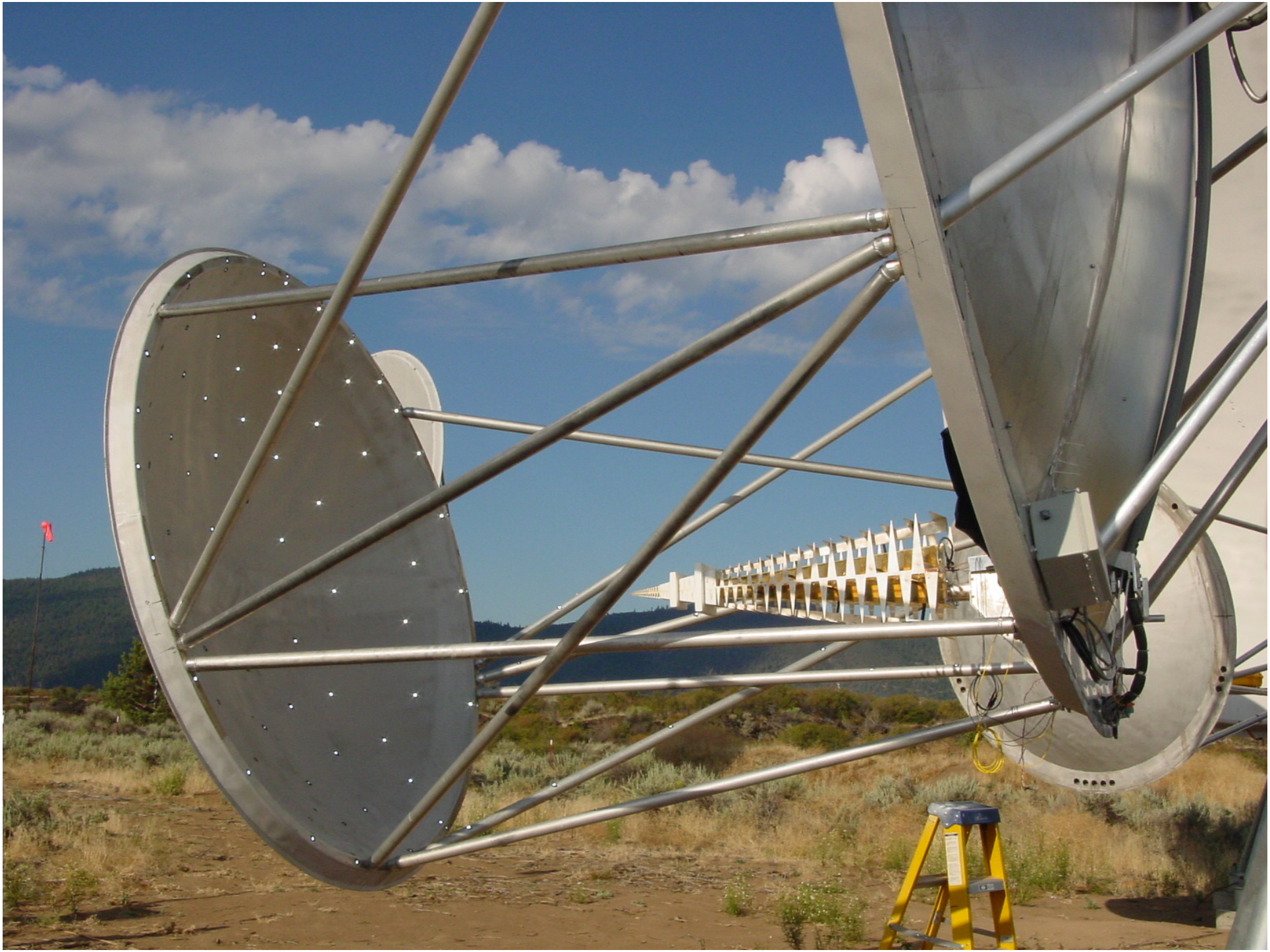

MWA
XNTD
PAPER
FAST
PAST
LAR
LWA
meerkat
karoo array telescope
CARMA
Combined Array for Research in Millimeter-Wave Astronomy
SKA
SQUARE KILOMETRE ARRAY
LOFAR
Expanded
Very Large Array
LWA
ALMA
ATACAMA LARGE MILLIMETER ARRAY

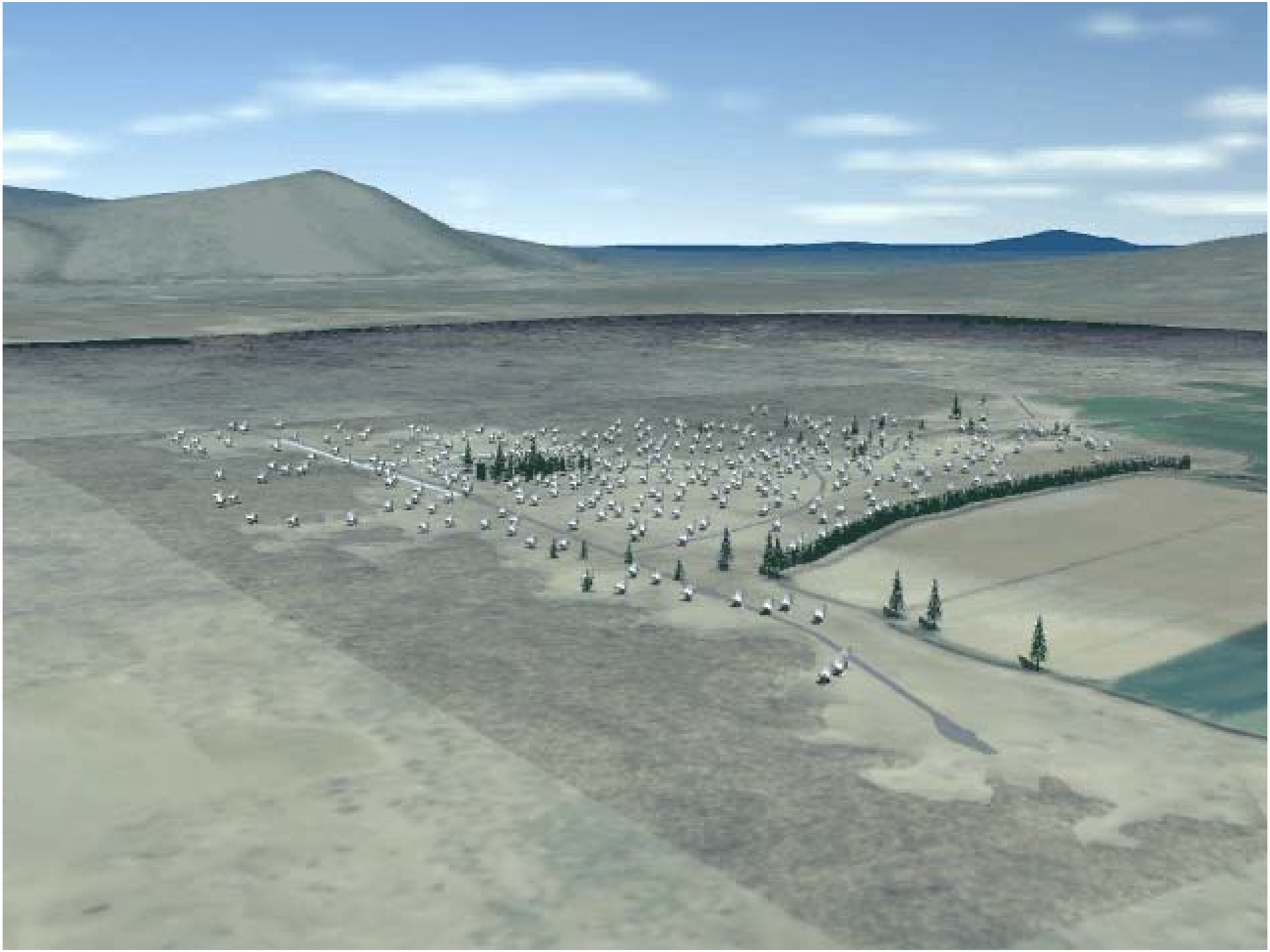

xilostudios.com

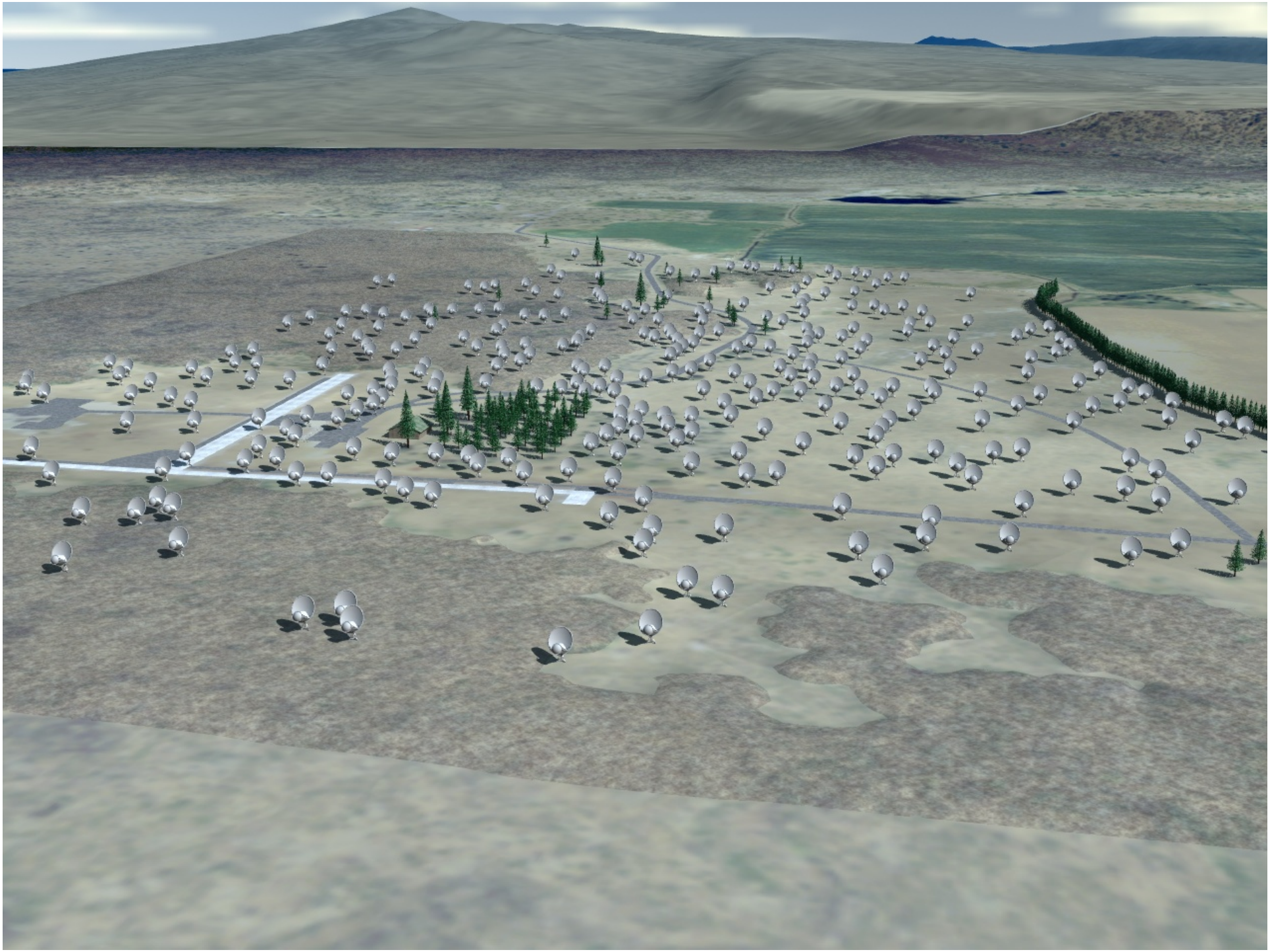
Allen Telescope Array



- 6.1-meter offset Gregorian (2.4-meter secondary)
- rim-supported, hydroformed dishes



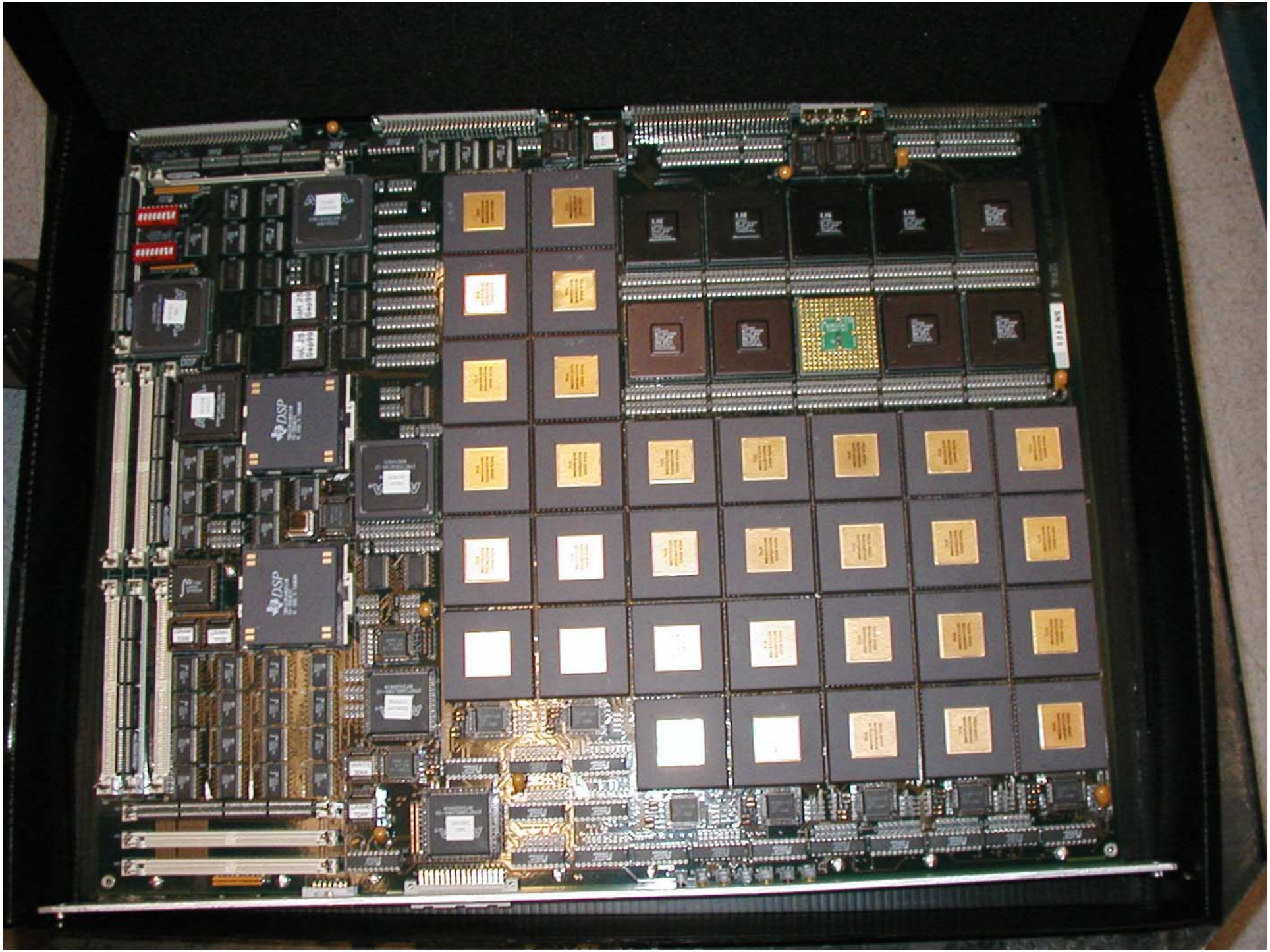




ATA-42 Operational October 2007

The Problem with the Current Hardware Development Model

- Takes 5 to 10 years
- Cost Dominated by NRE because of custom Boards, Backplanes, Protocols
- Antiquated by the time it's released.
- How to buy the hardware at the last minute?
- Each observatory designs from scratch


DSP
DSP


CAUTION
WERNER

CASPER Real-time Signal Processing Instrumentation
(NSF ATI, MRI)

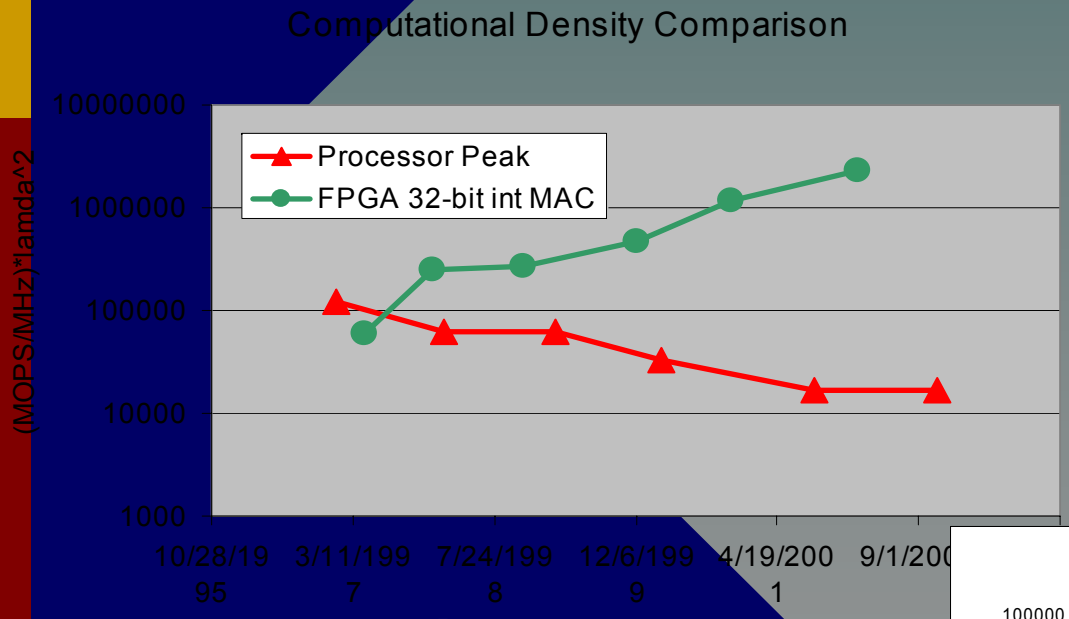
- Low NRE, shared by the community
- Rapid development (12 instruments / 2 years)
- Open-source, collaborative
- Reusable, platform-independent gateware
- Modular, upgradeable hardware
- Industry standard communication protocols
- Use switches to solve correlator interconnect
- Low Cost

Solution:

- Modular Hardware
  - Low number of board designs
  - Can be upgraded piecemeal or all together
  - Reusable
  - Standard signal processing model which is consistent between upgrades.

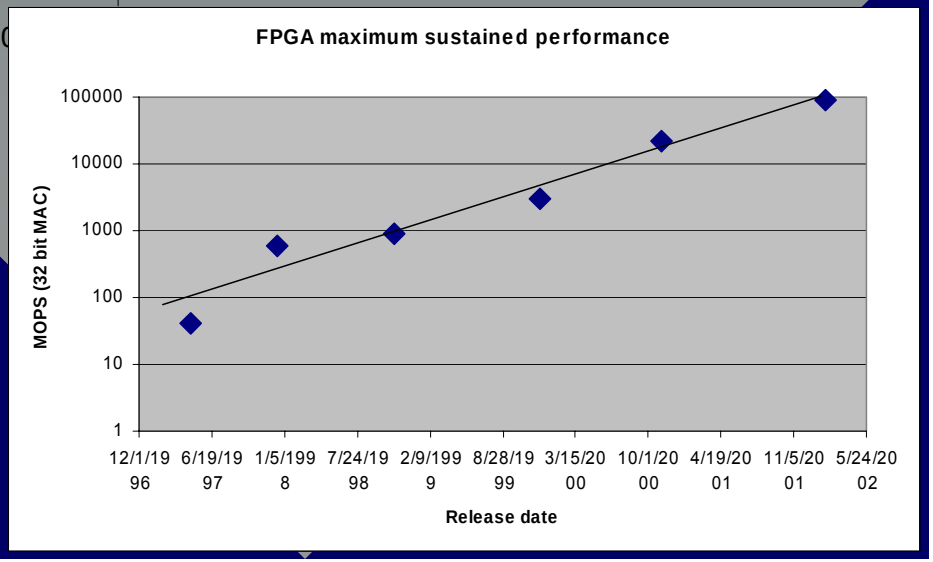
Solution: use FPGA's

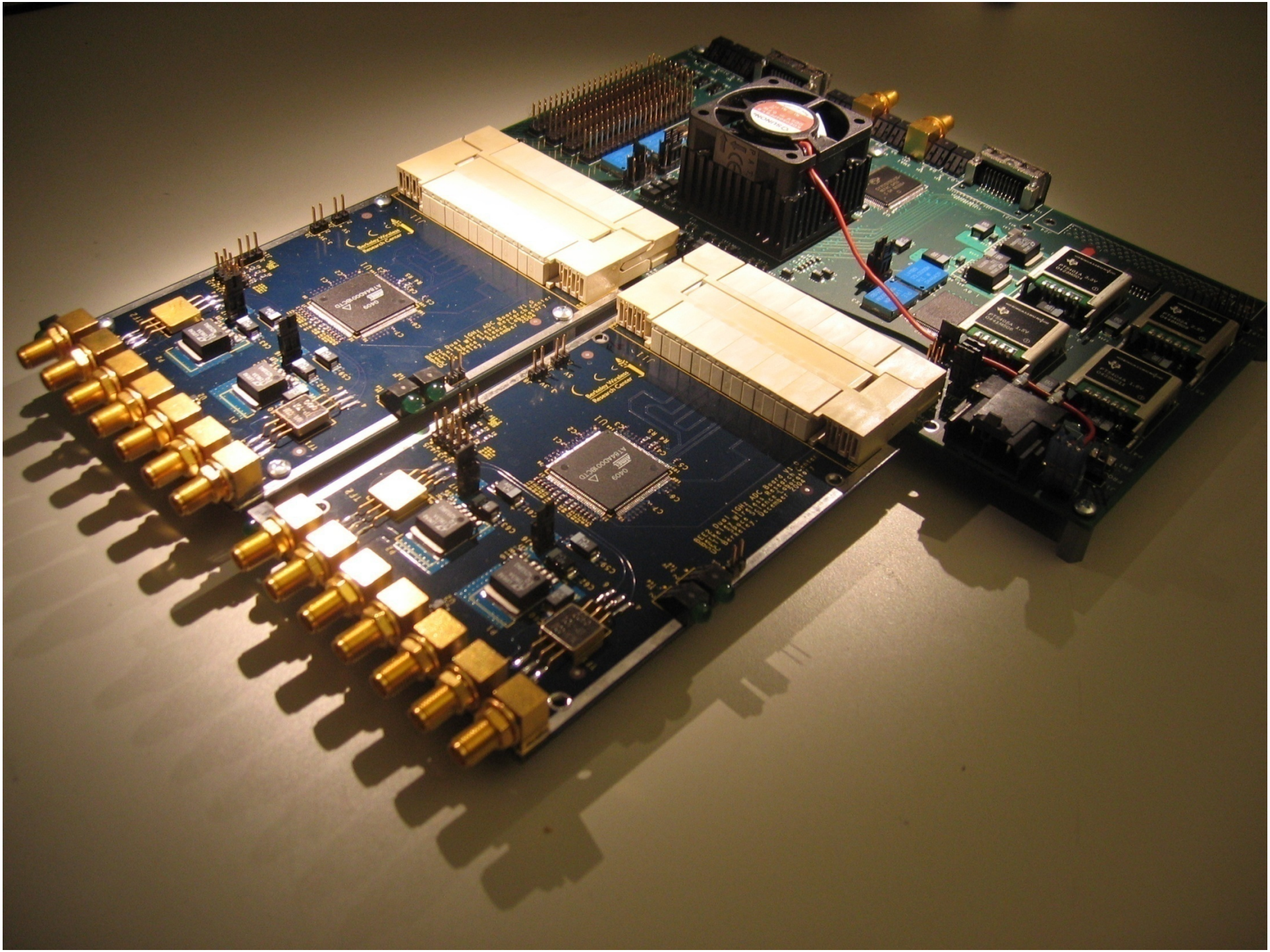
1 FPGA = 100 Pentium, 1/500 the power per op

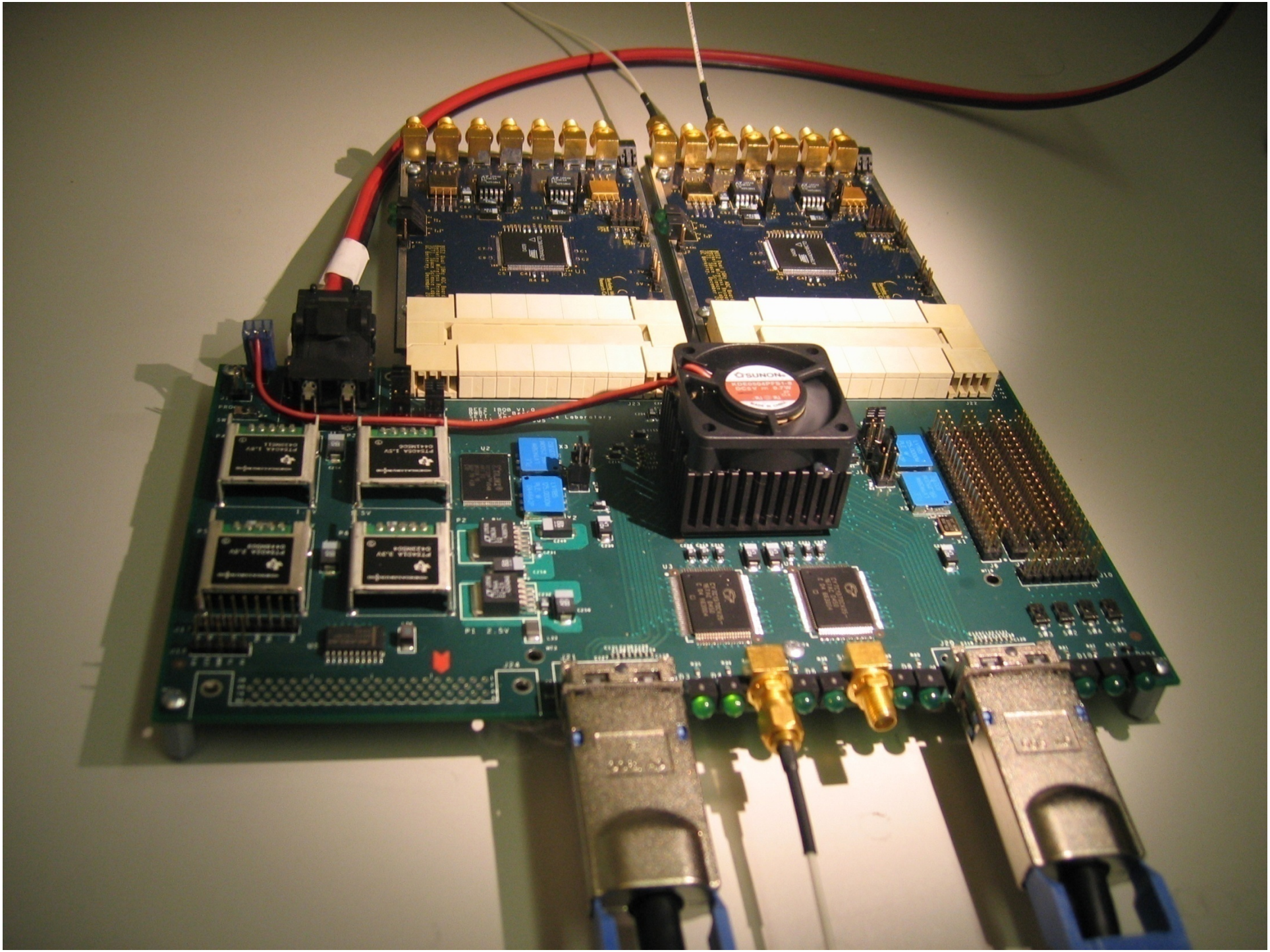


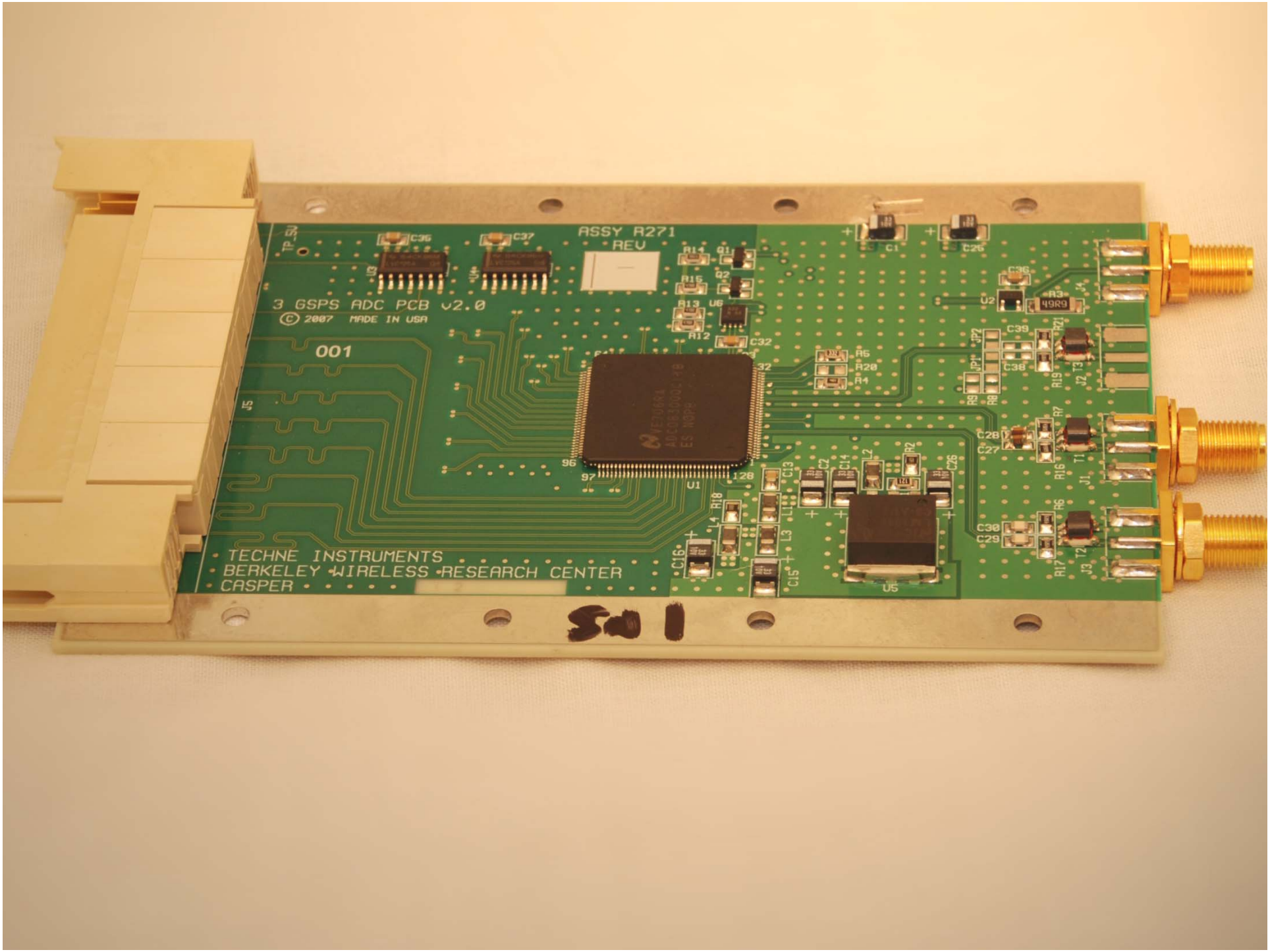
Moores Law for FGPA's

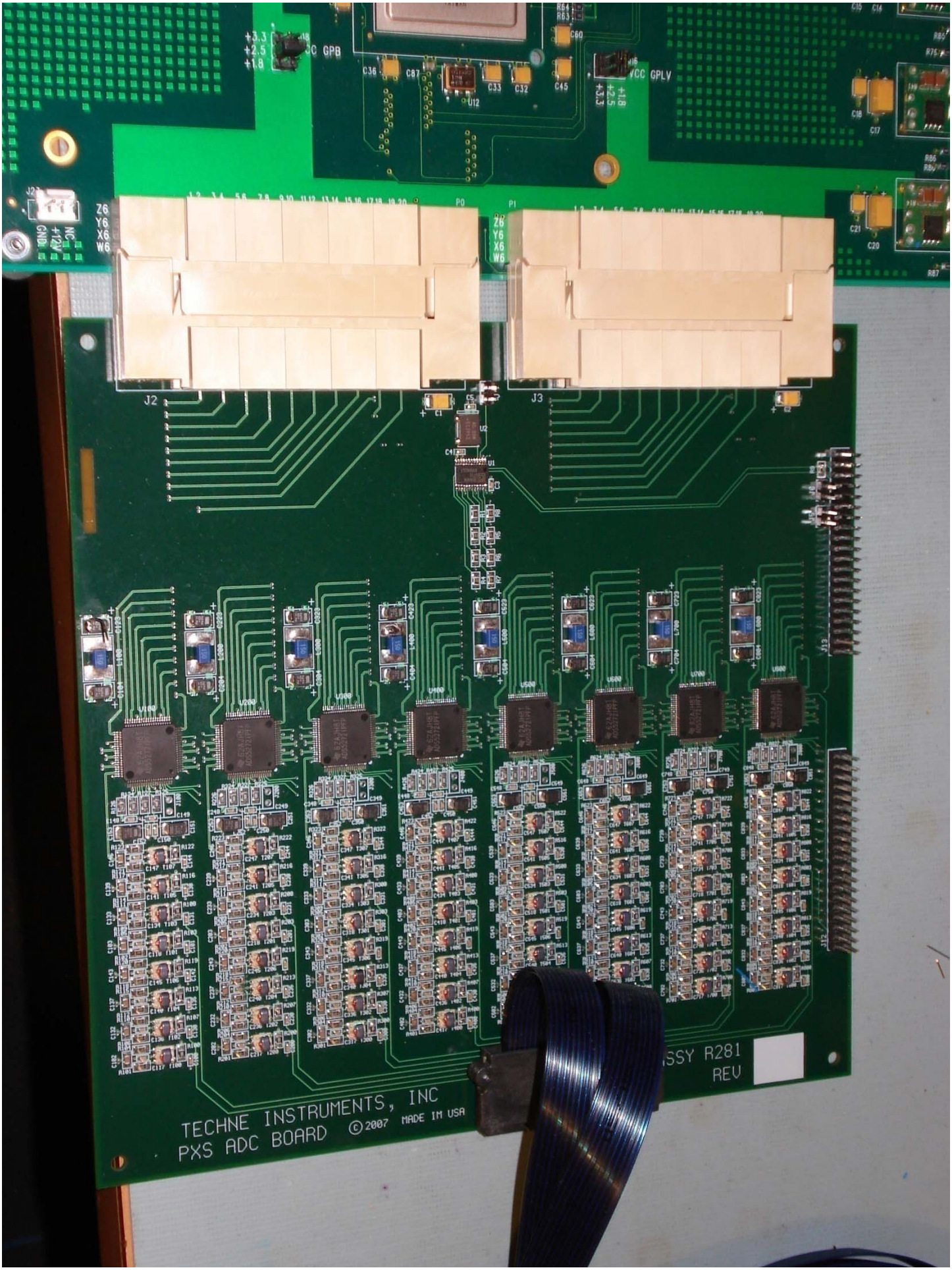
3X improvement per year!








ASSY R271
REV
3 GSPS ADC PCB v2.0
© 2007 MADE IN USA
001
TECHNE INSTRUMENTS
BERKELEY WIRELESS RESEARCH CENTER
CASPER
Sn 1


TECHNE INSTRUMENTS, INC
PXS ADC BOARD ©2007 MADE IM USA
REV
J2
J3
P0
P1

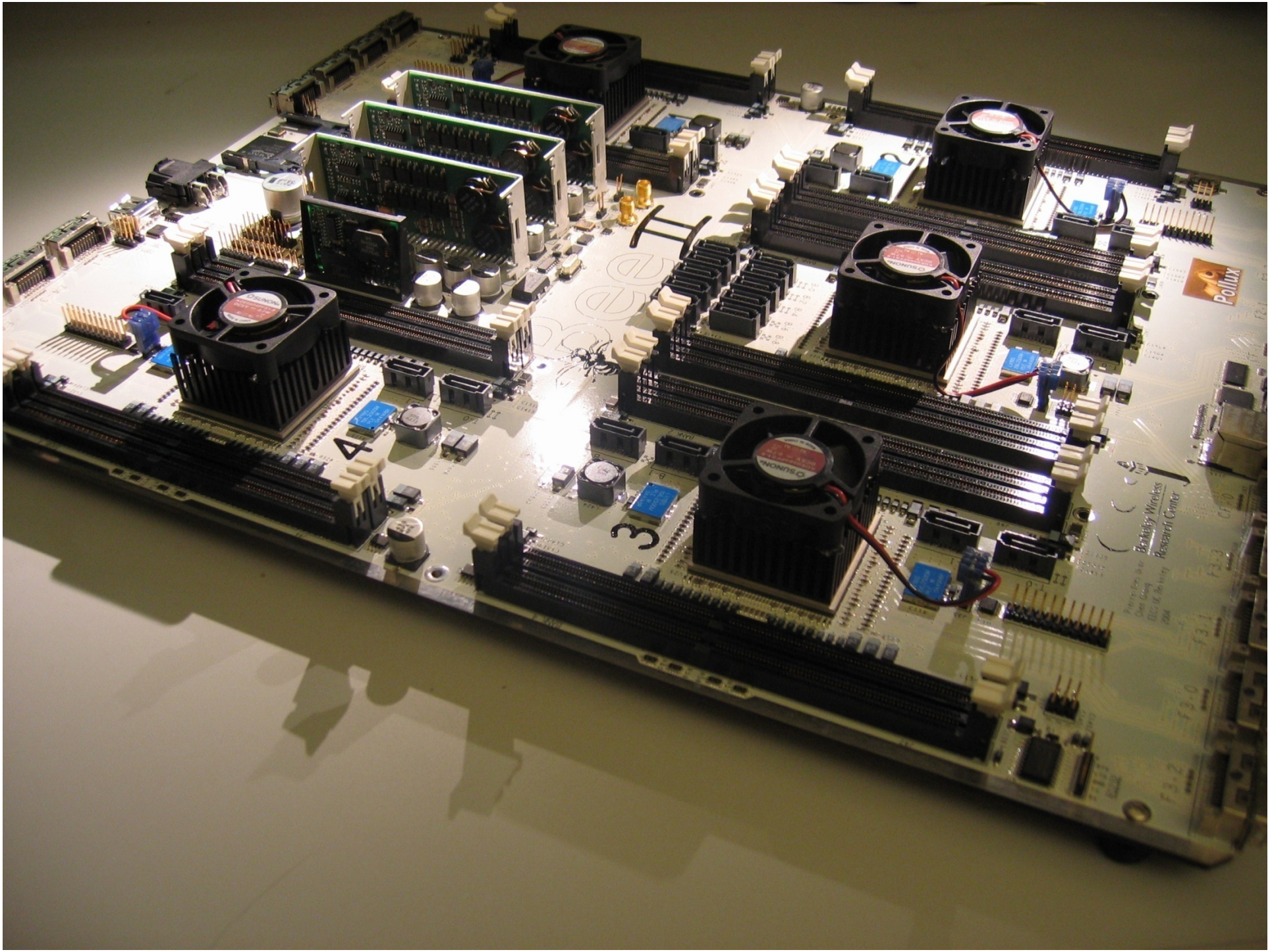
Agilent ADC-FGPA-CX4 board ?

20 Gsps 8 bit Agilent ADC

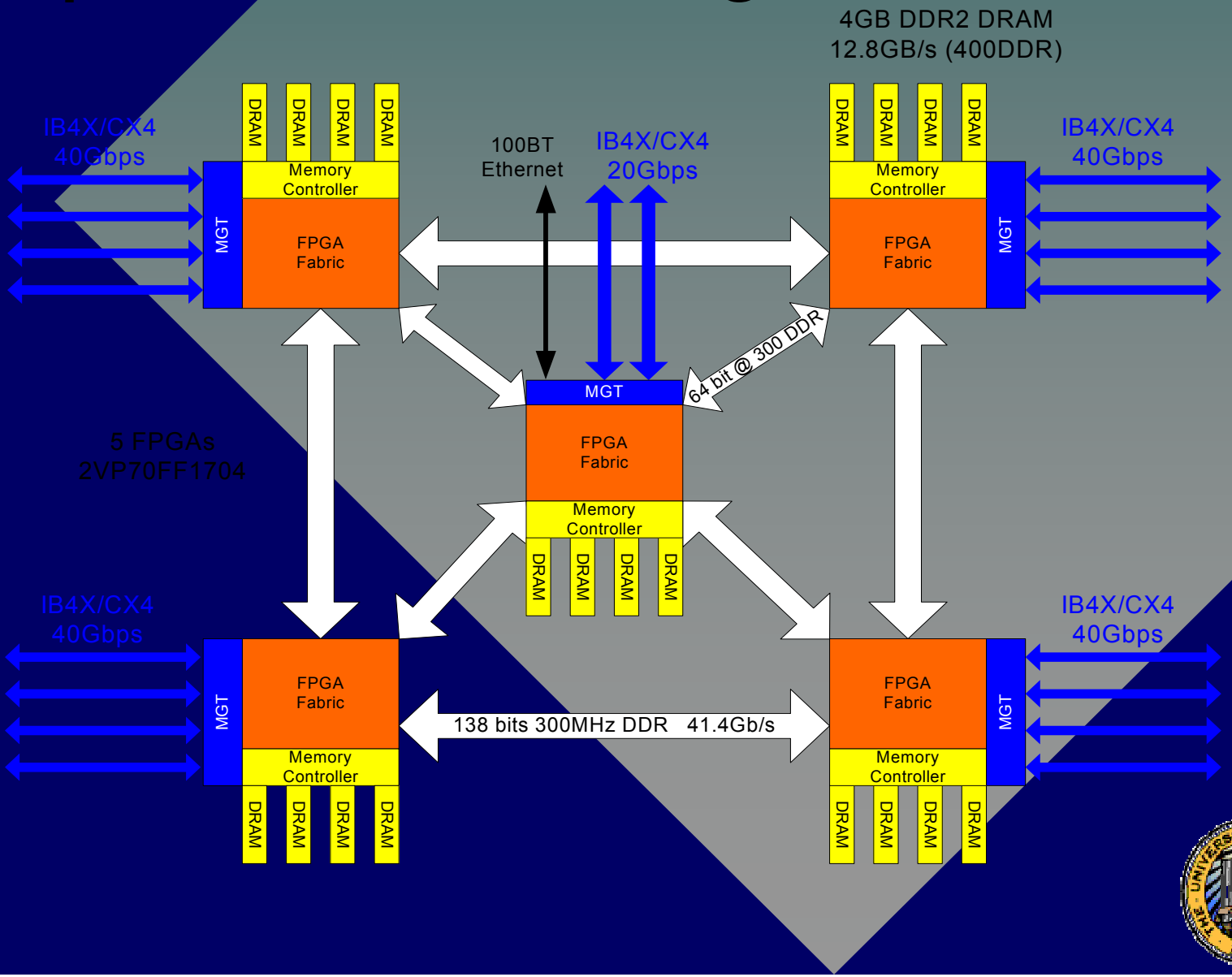
XC5VSX240T

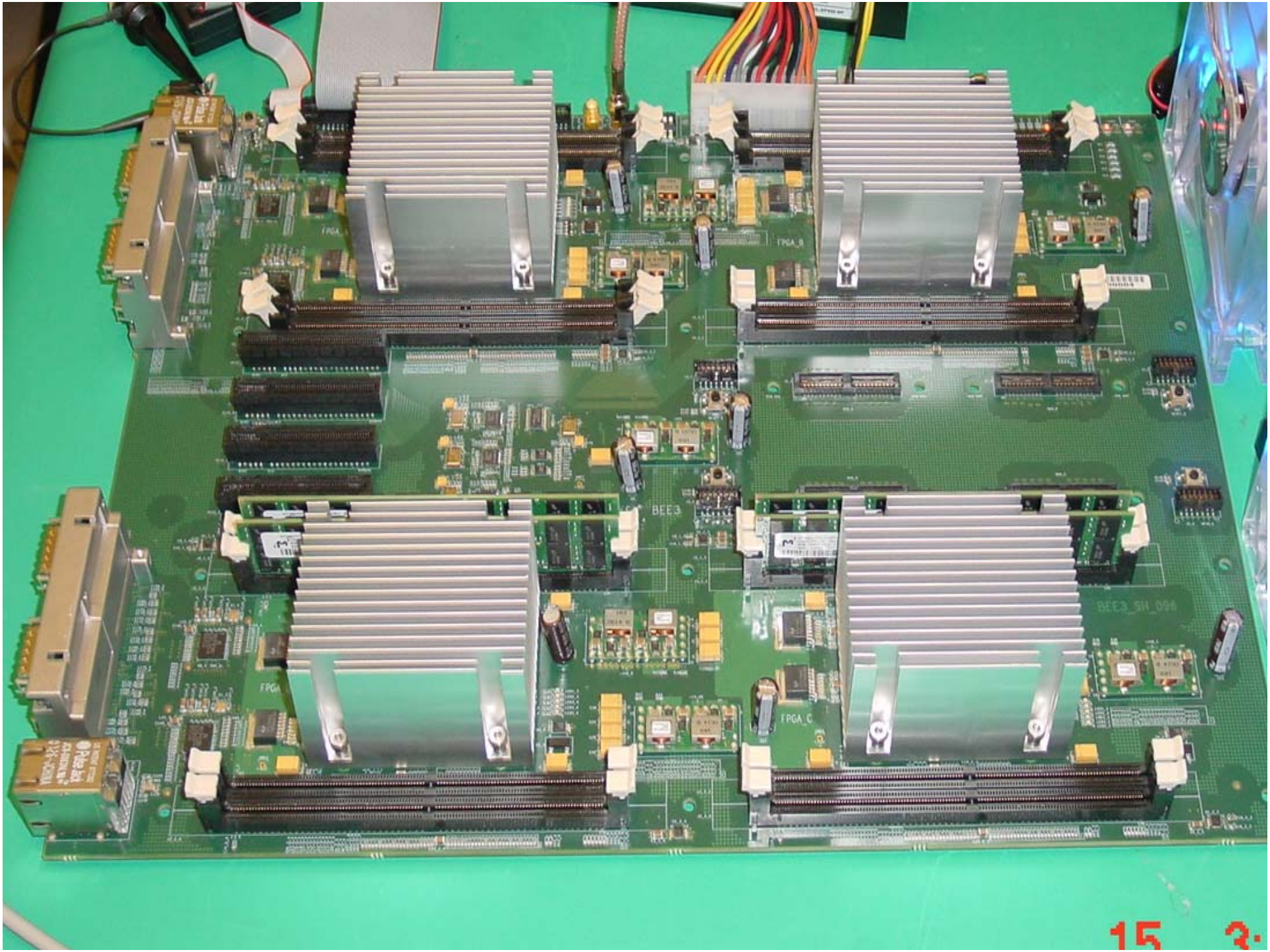
6 CX4 ports

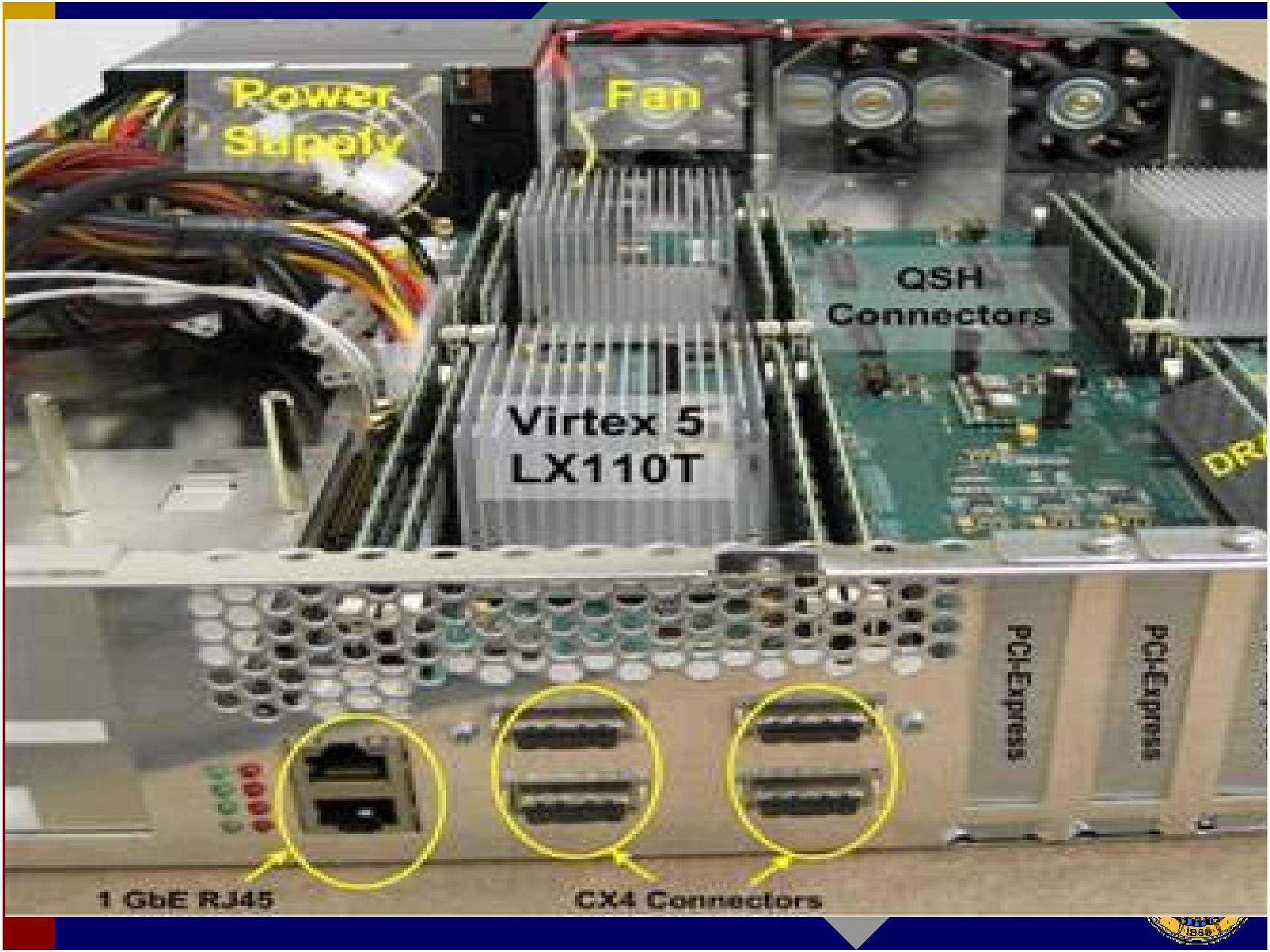
120 Gbps xaui
100 Gbps infiniband
60 Gbps 10 Gbe

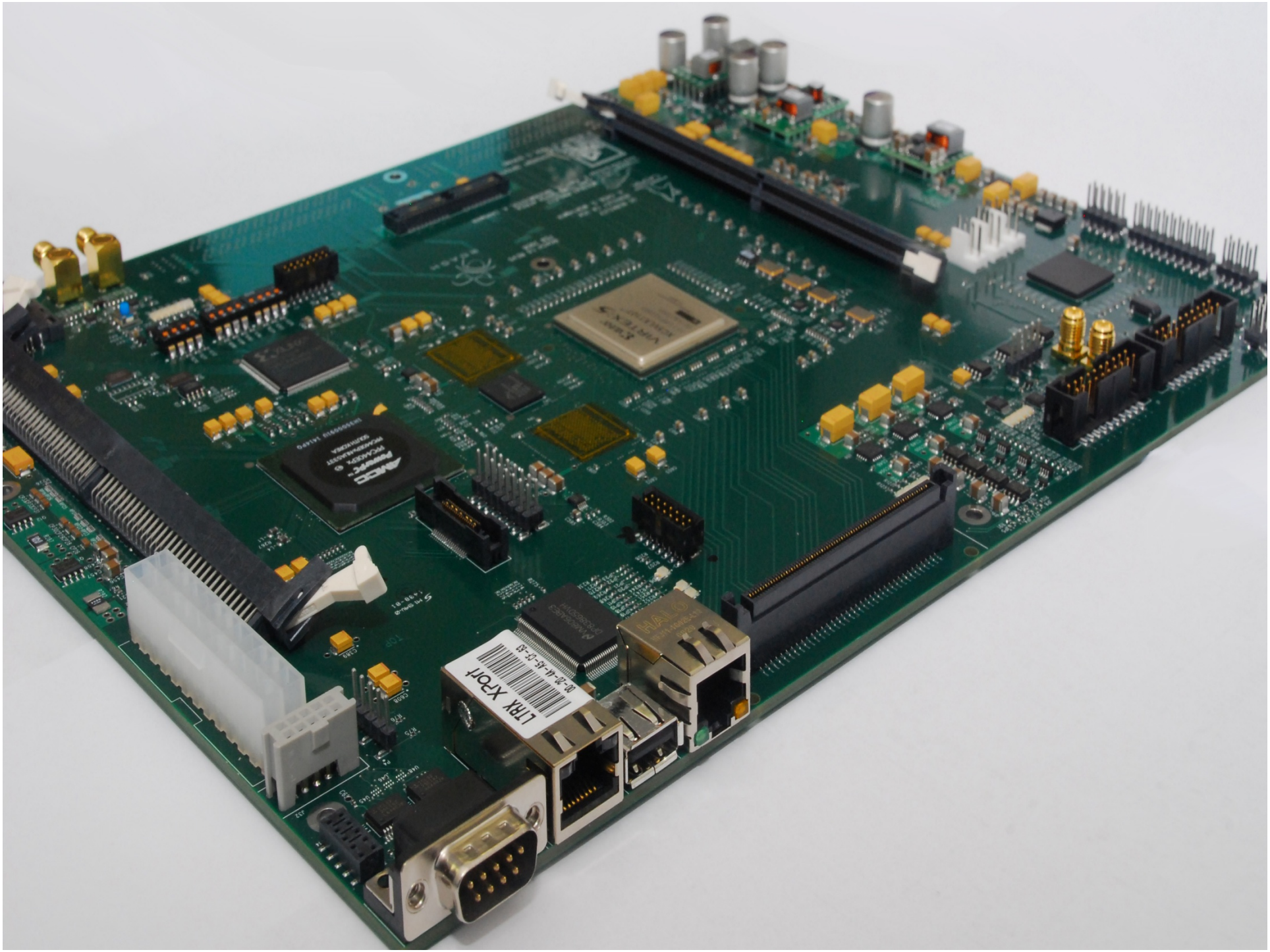

Pollux
Berkeley Wireless
Research Center

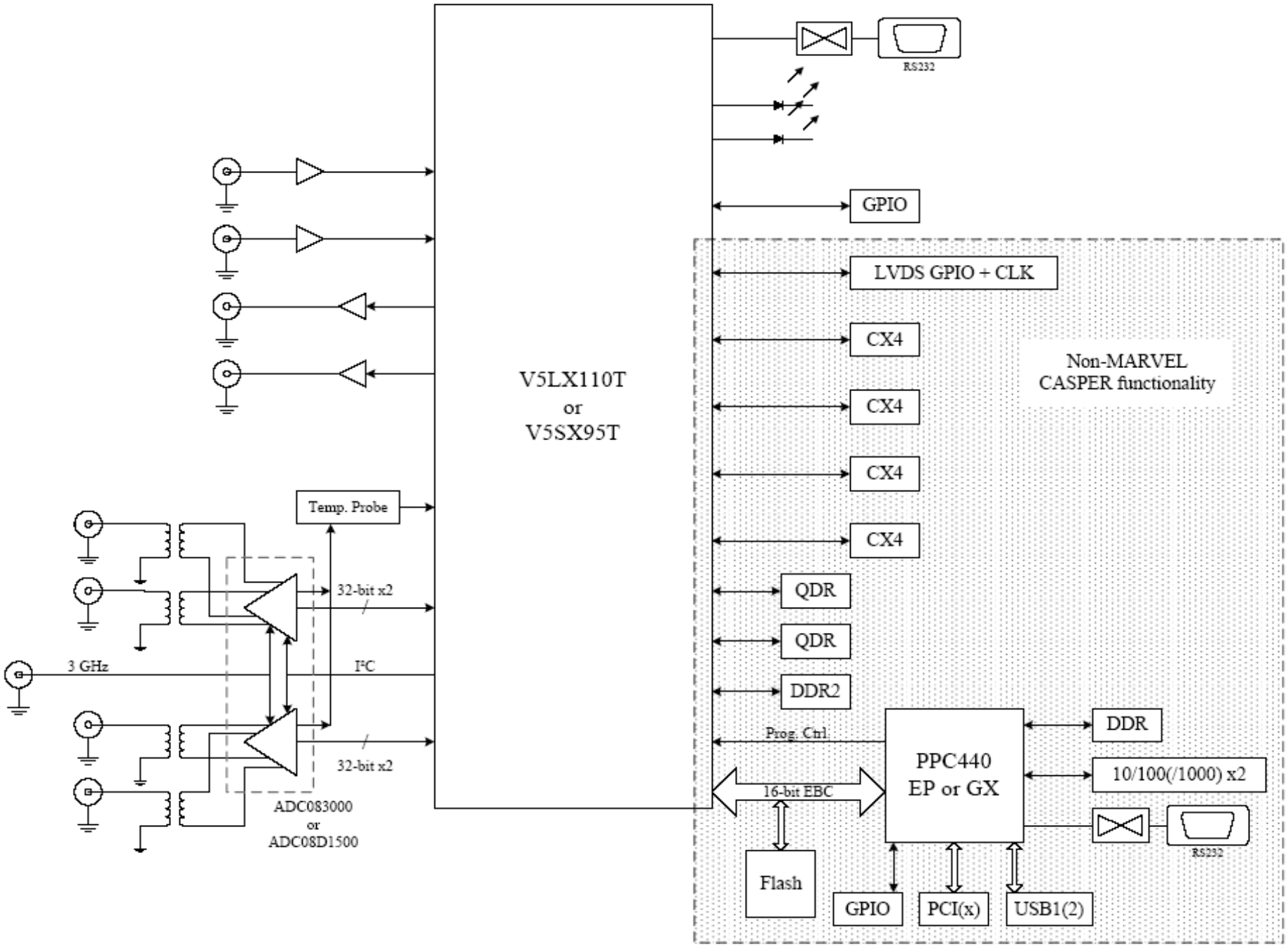
Compute Module Diagram




FPGA_B
BEE3
FPGA_C
15 3·


Power Supply
Fan
QSH Connectors
Virtex 5 LX110T
PCI-Express
PCI-Express
1 GbE RJ45
CX4 Connectors


LTRX XPort
00-20-4A-A5-67-A3


RS232
GPIO
LVDS GPIO + CLK
CX4
CX4
CX4
CX4
Non-MARVEL
CASPER functionality
V5LX110T
or
V5SX95T
Temp. Probe
32-bit x2
3 GHz
I²C
32-bit x2
ADC083000
or
ADC08D1500
QDR
QDR
DDR2
Prog. Ctrl
16-bit EBC
PPC440
EP or GX
DDR
10/100(/1000) x2
RS232
Flash
GPIO
PCI(x)
USB1(2)

Board Interconnect - Upgradable

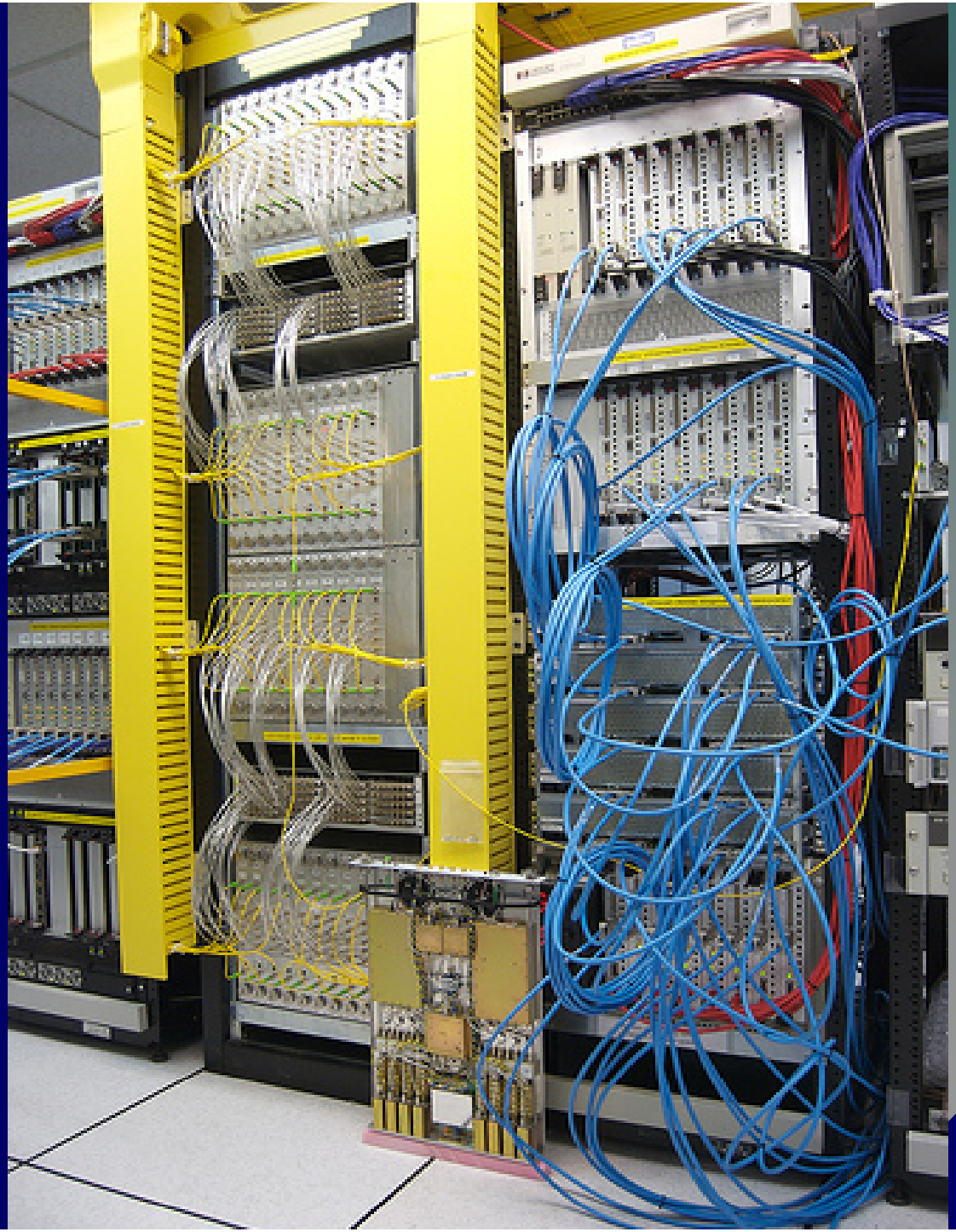
- Problem: Backplanes are short lived

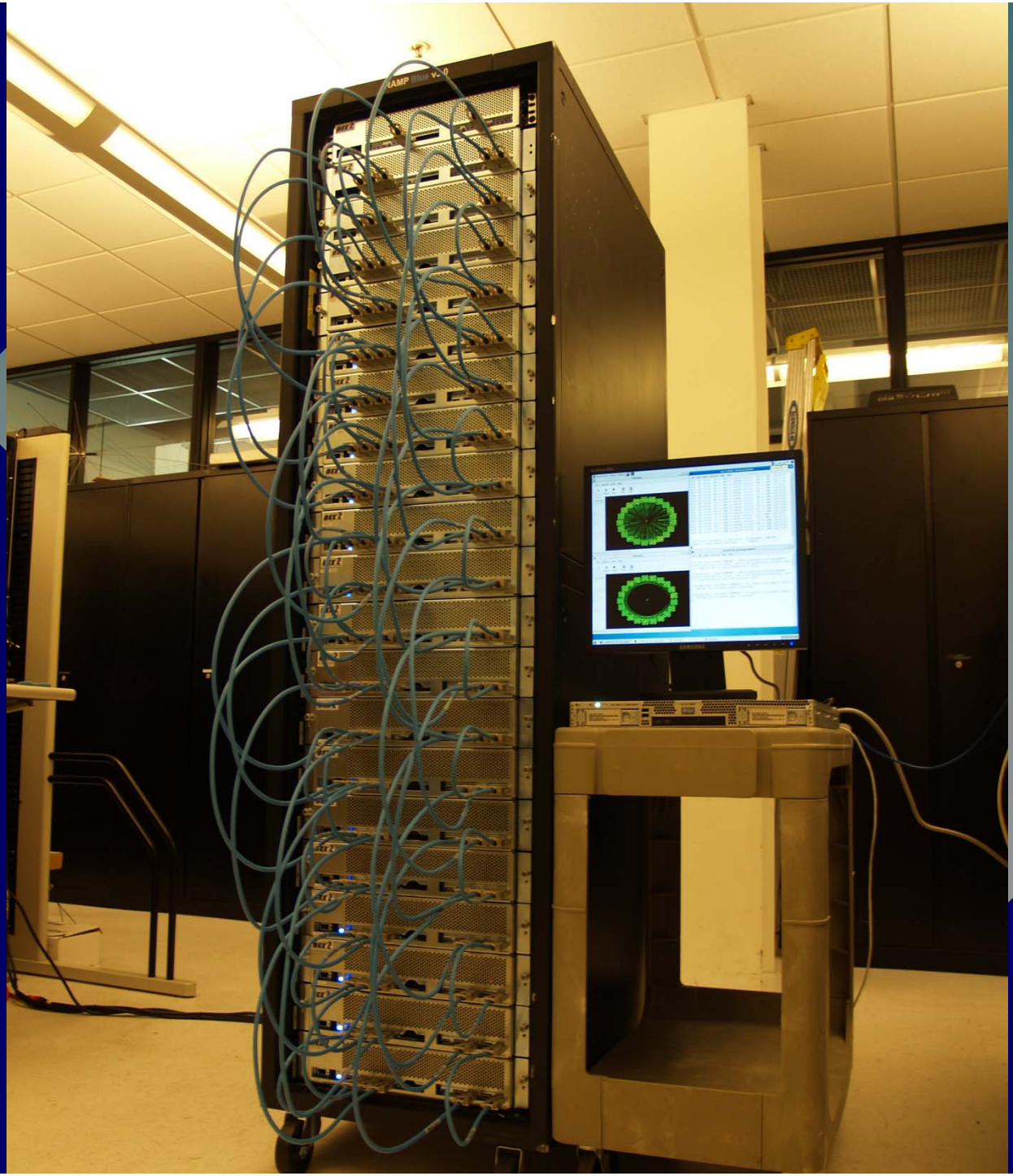
  (S100, Multibus, VME, ISA, EISA, PCI, PCIx, PCIe, compactPCI, compactPCIe, ATCA...)

- Solution: Use 10Gbit Ethernet

  (10Gbe, Infiniband, Myrinet, Xaui, Aurora)

  Copper CX4 (40 meters max) or Optical



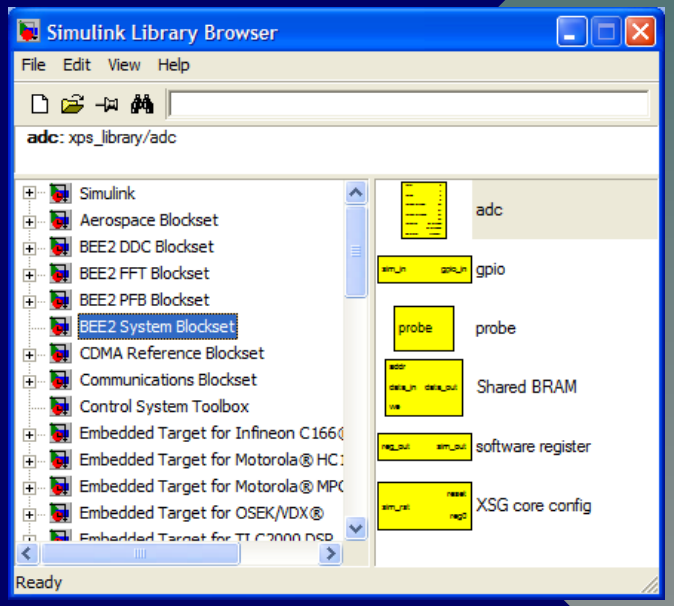


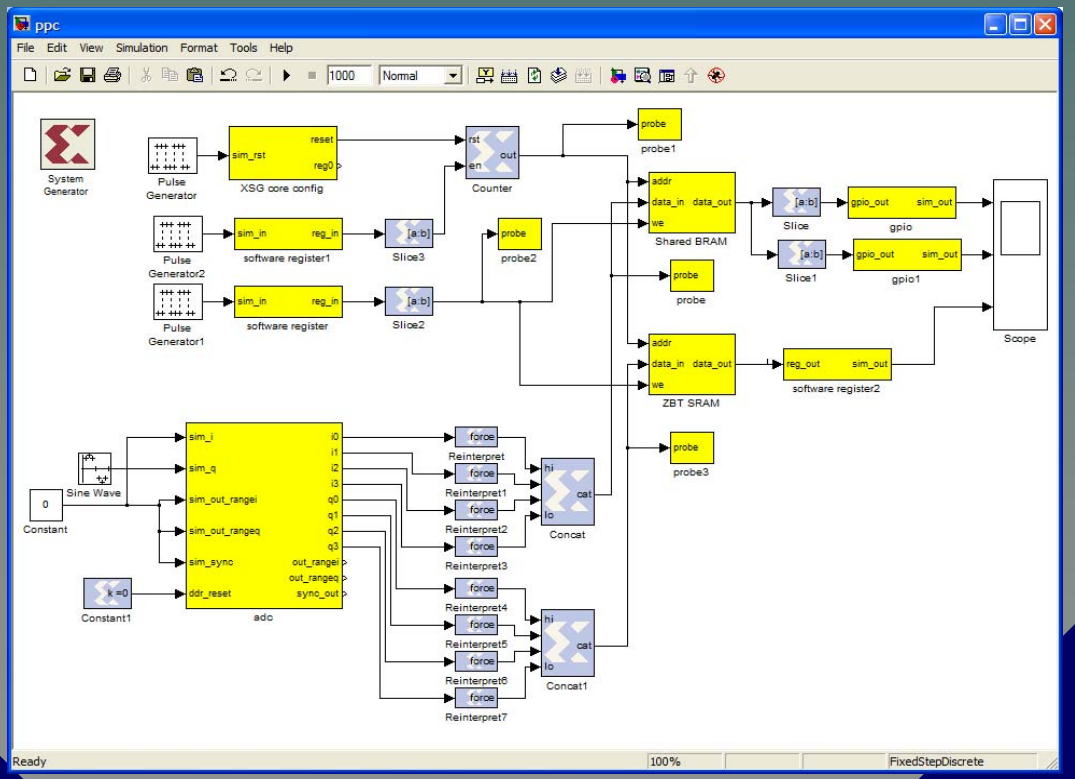
Platform-Independent, Parameterized Gateware

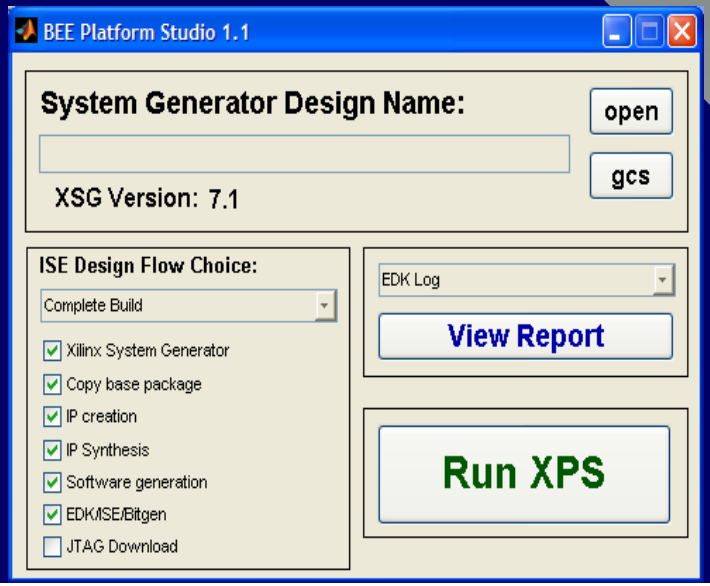
- What is Gateware?
  - Design logic of FPGAs

    (between hardware and software)
- Need libraries for signal processing which don't have to be rewritten every hardware generation.
- Matlab Simulink!
- LINUX file I/O and process control (Borph)

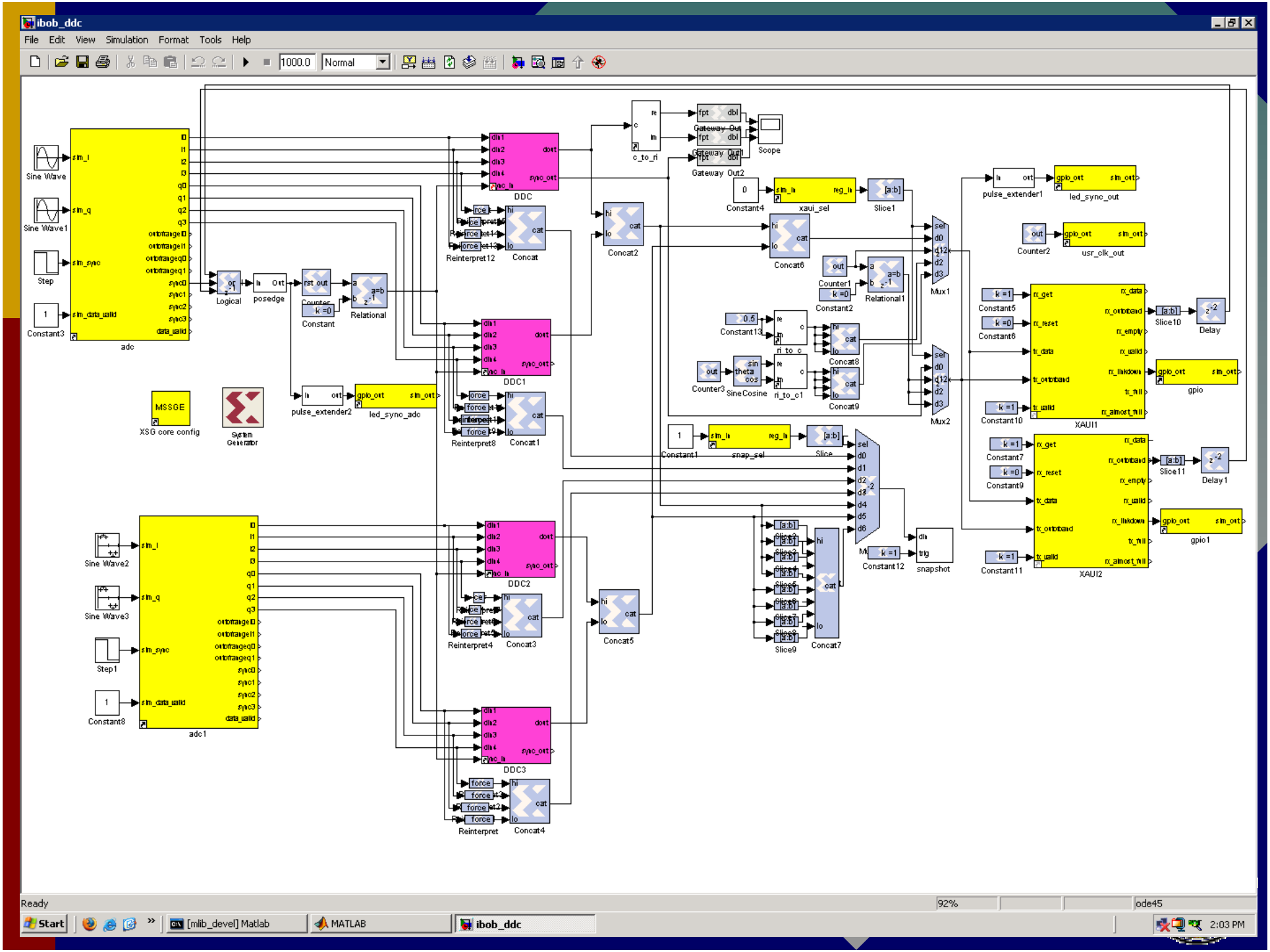
Simulink-based Design Tool Flow





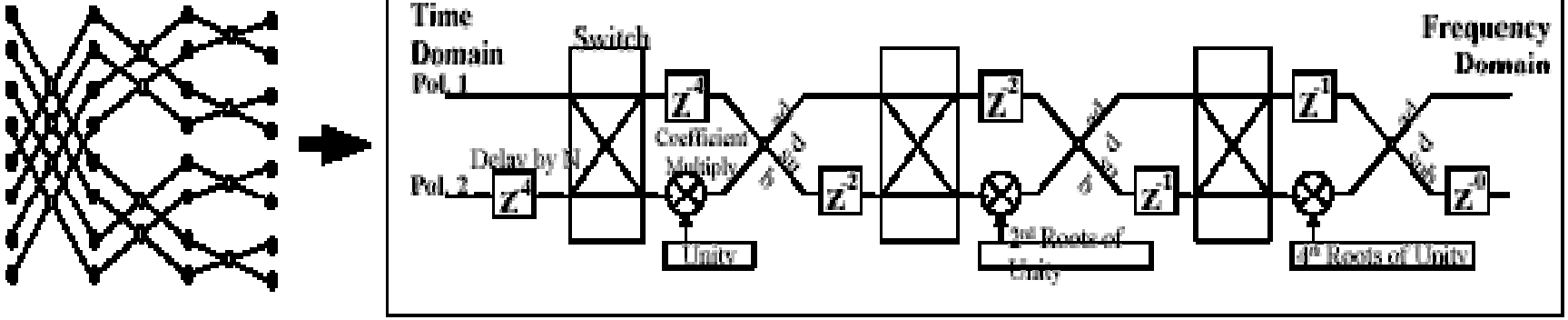


- Simulink Xilinx System Generator Library
- Custom BEE2 Library Blocksets
- Software programmable registers
- BEE Platform Studio


ibob_ddc
File Edit View Simulation Format Tools Help
Normal
Sine Wave
Sine Wave1
Step
Constant3
adc
Logical
posedge
Counter
Constant
Relational
DDC
DDC1
DDC2
DDC3
Reinterpret12
Concat
Reinterpret8
Concat1
Reinterpret4
Concat3
Reinterpret
Concat4
c_to_ri
Gateway Out
Gateway Out1
Gateway Out2
Scope
Concat2
Concat5
Constant4
xaui_sel
Slice1
Concat6
Counter1
Constant2
Relational1
Mux1
Constant13
ri_to_c
Concat8
Counter3
SineCosine
ri_to_c1
Concat9
Mux2
Constant1
snap_sel
Slice
Mux
Constant12
snapshot
Slice9
Concat7
pulse_extender1
led_sync_out
Counter2
usr_clk_out
Constant5
Constant6
Slice10
Delay
XAUI1
gpio
Constant10
Constant7
Constant9
Slice11
Delay1
XAUI2
gpio1
Constant11
MSSGE
XSG core config
System Generator
pulse_extender2
led_sync_adc
Sine Wave2
Sine Wave3
Step1
Constant8
adc1
Ready
92%
ode45
Start
[mlib_devel] Matlab
MATLAB
ibob_ddc
2:03 PM

Biplex Pipelined FFT

(Lynn Urry, Aaron Parsons, David MacMahon, Jeff Mock, JPL)

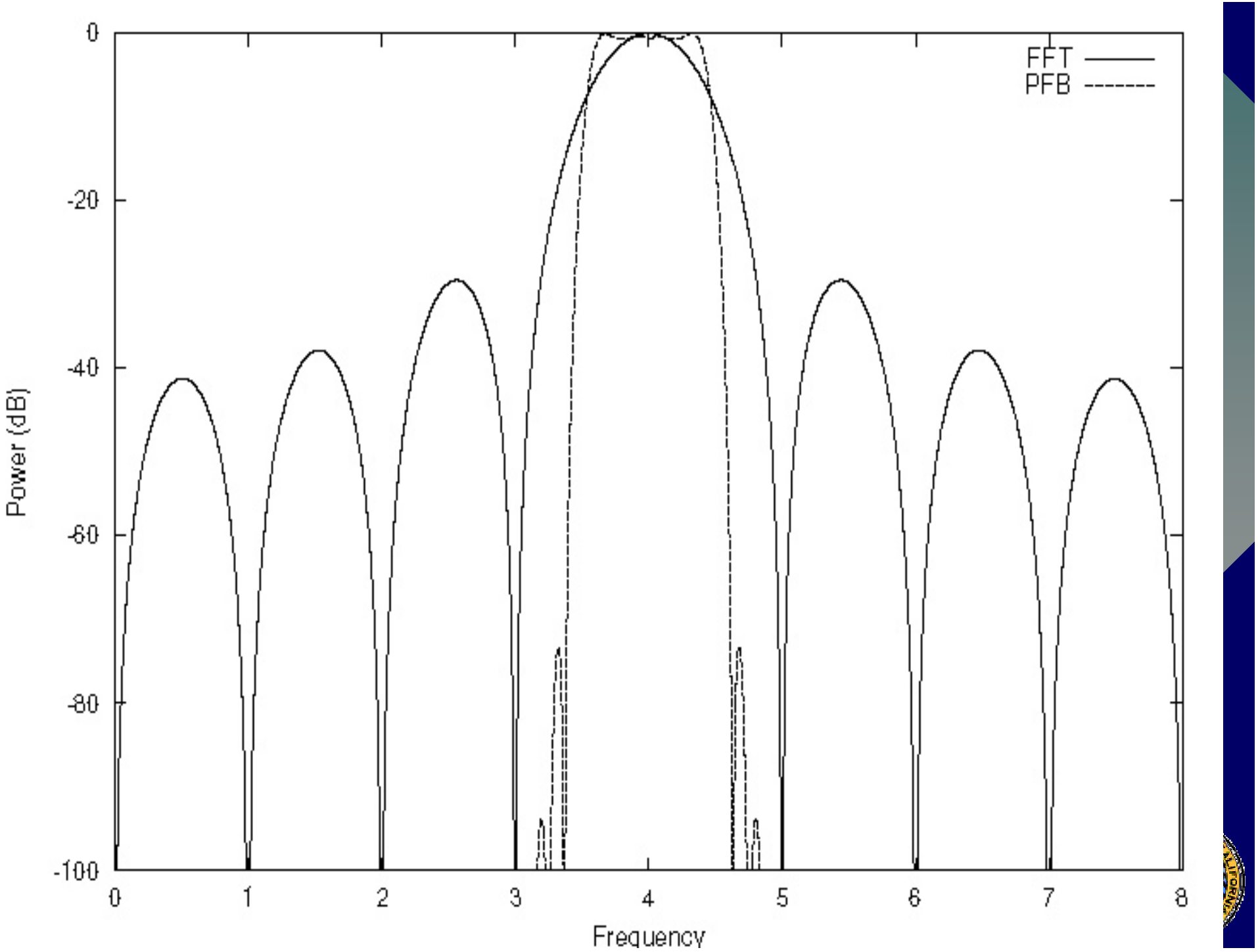


- Uses 1/6 the resources of the Xilinx module.

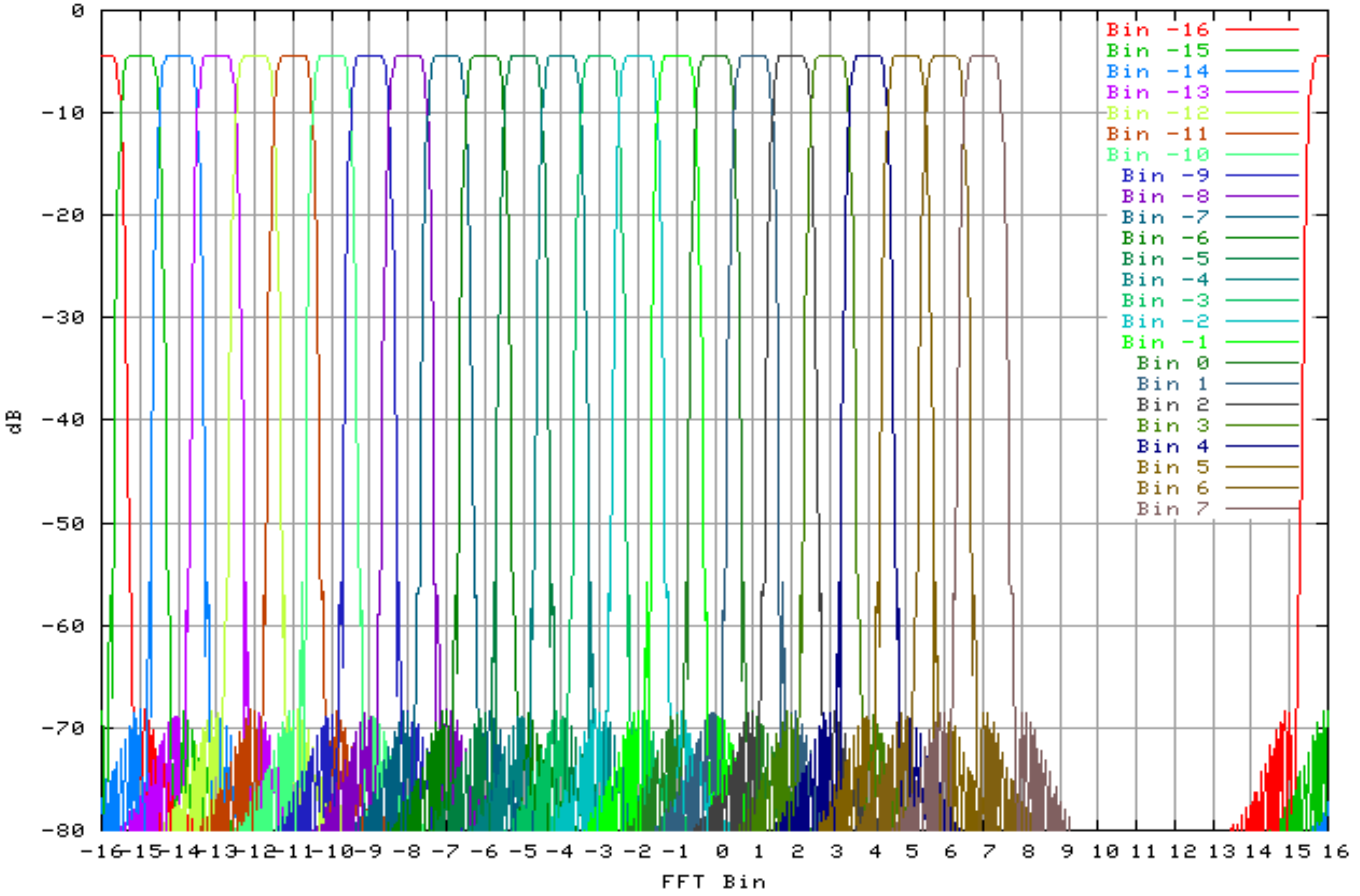
FFT controls

Simulink Library – Aaron Parsons, David MacMahon
Verilog Library – Jeff Mock

- Transform length
- Bandwidth
- Complex or Real
- Number of Polarizations
- Input bit width and output bit width
- twiddle coefficient bit width
- Run-time programmable down-shifting
- Decimate option


FFT
PFB
Power (dB)
Frequency
0
-20
-40
-60
-80
-100
0
1
2
3
4
5
6
7
8

PFB vs. FFT


dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-16 -15 -14 -13 -12 -11 -10 -9 -8 -7 -6 -5 -4 -3 -2 -1 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
FFT Bin
Bin -16
Bin -15
Bin -14
Bin -13
Bin -12
Bin -11
Bin -10
Bin -9
Bin -8
Bin -7
Bin -6
Bin -5
Bin -4
Bin -3
Bin -2
Bin -1
Bin 0
Bin 1
Bin 2
Bin 3
Bin 4
Bin 5
Bin 6
Bin 7

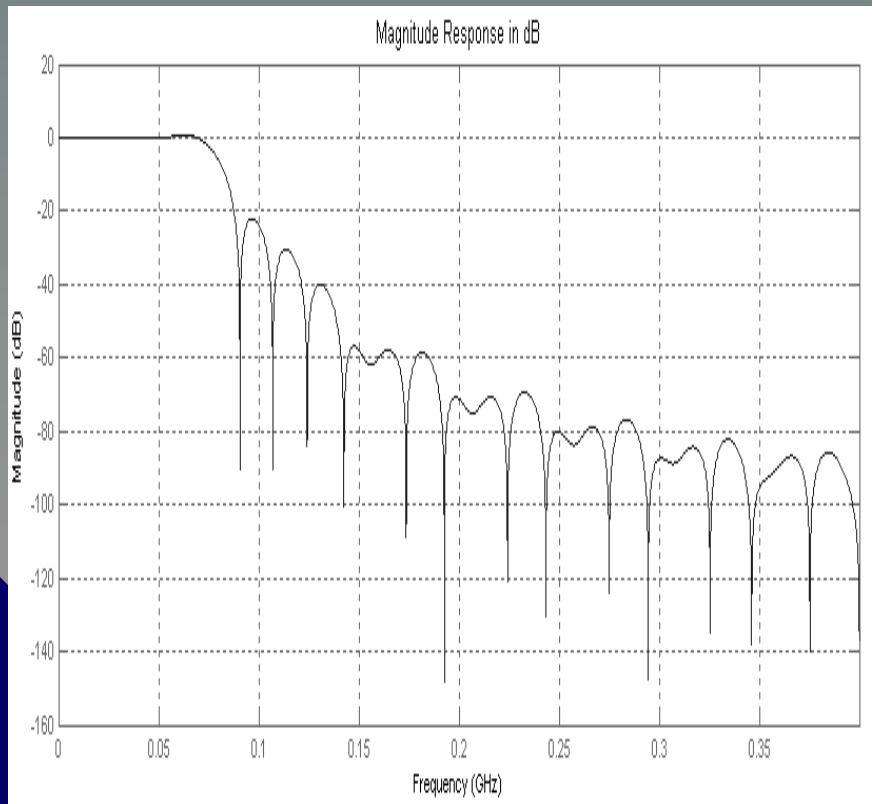
Additional PFB controls

(Aaron Parsons, Jeff Mock)

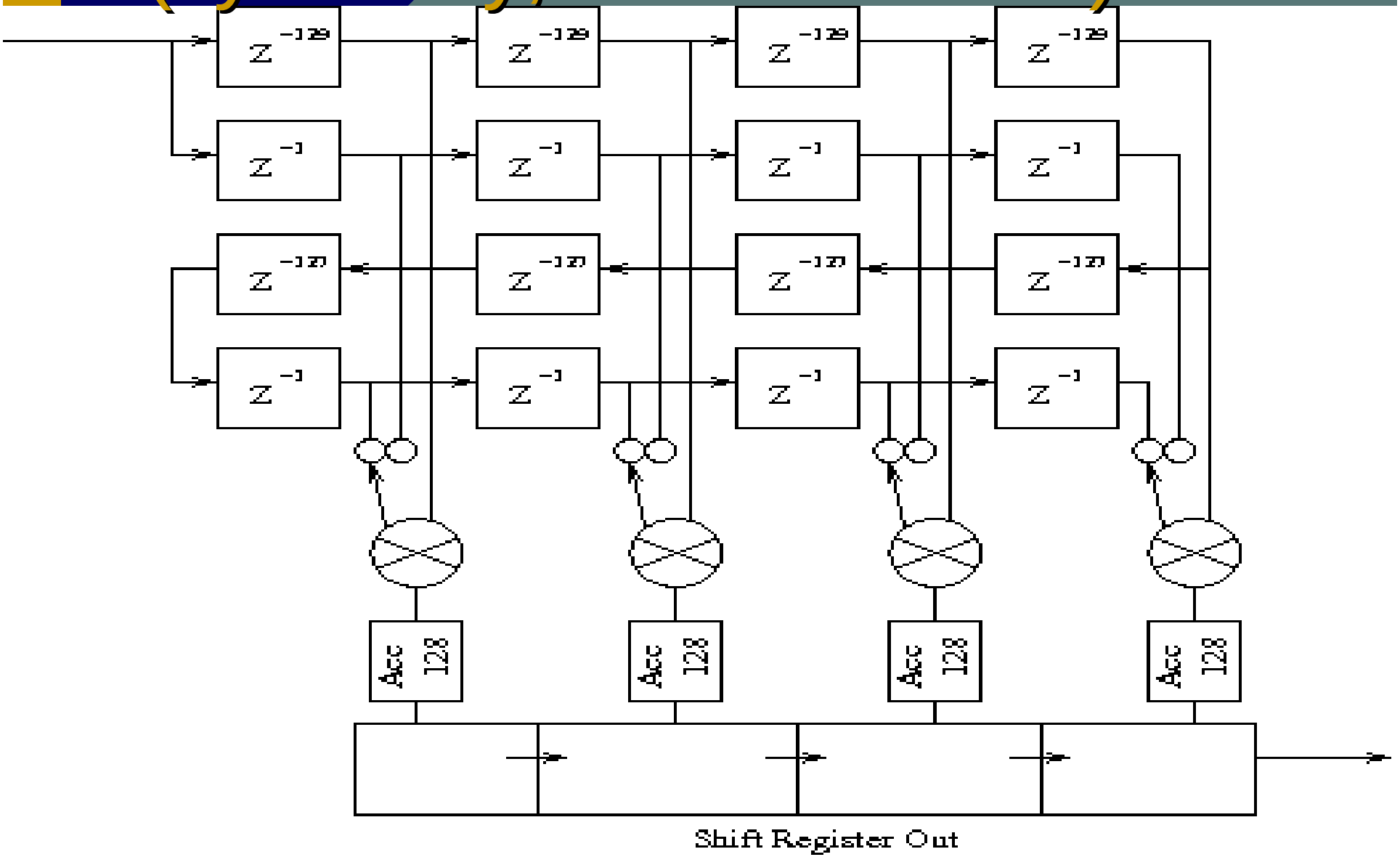
- Filter overlap
- Width of filter coefficients
- Window function for filter (hamming, hanning, etc.)
- Import filter coefficients for custom filter performance

Digital Down-Converter

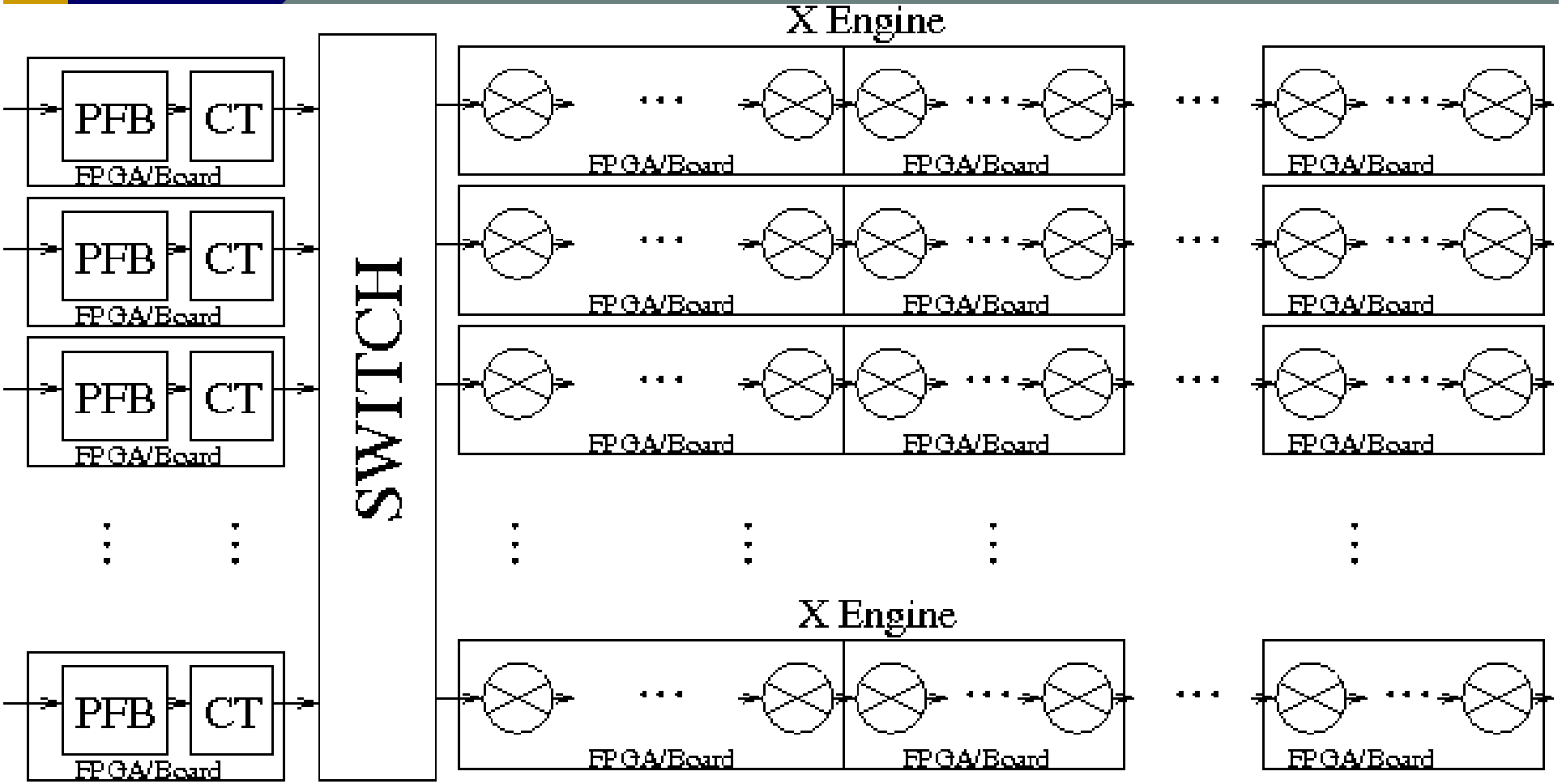
- Selectable # of FIR taps
- On-the-fly programmable mix frequency
- Selectable FIR coeff
- Agile sub-band selection.



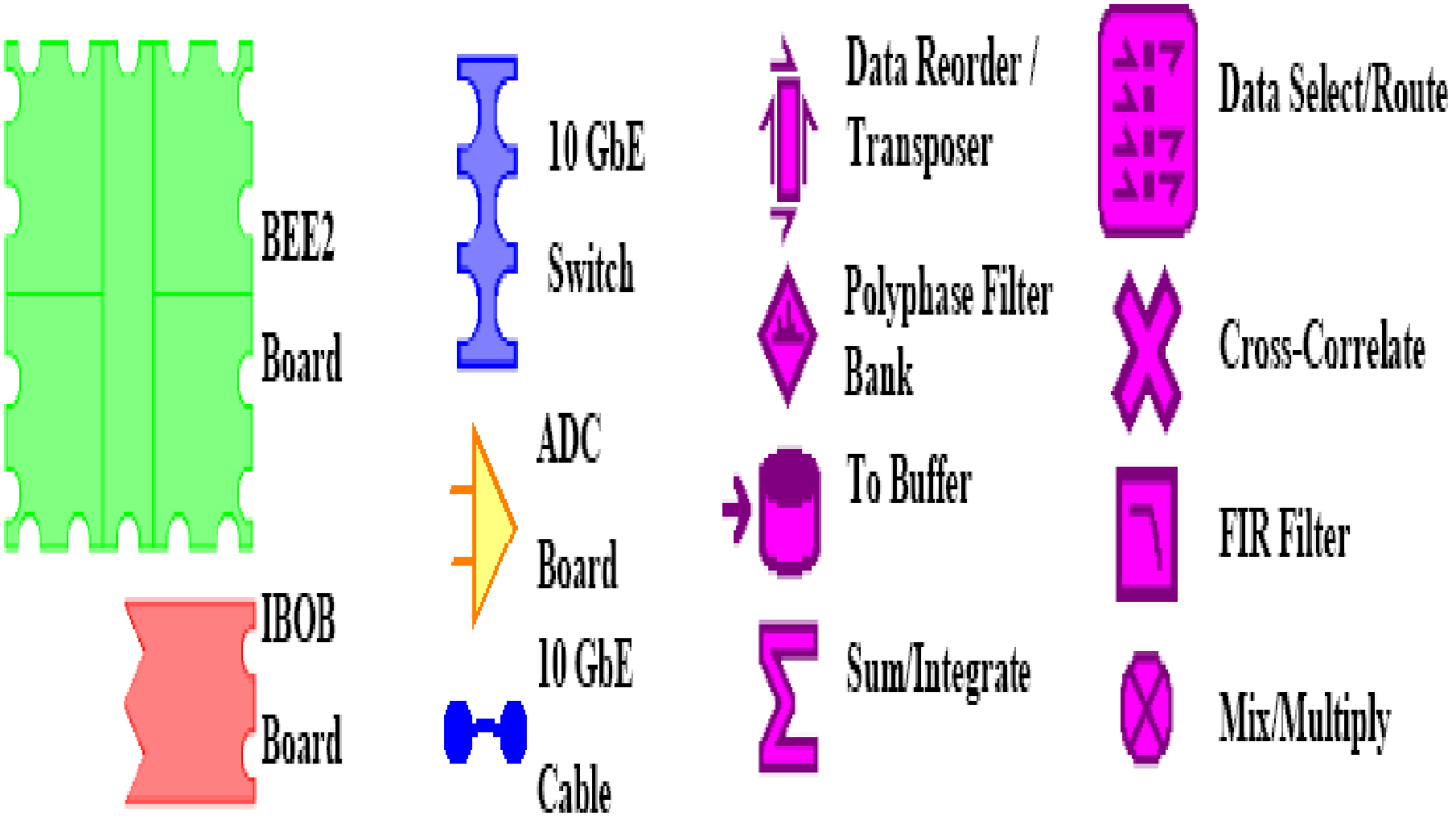
X-Engine Correlation Architecture (Lynn Urry, Aaron Parsons)



X-Engine Architecture: applied to an arbitrary sized antenna array

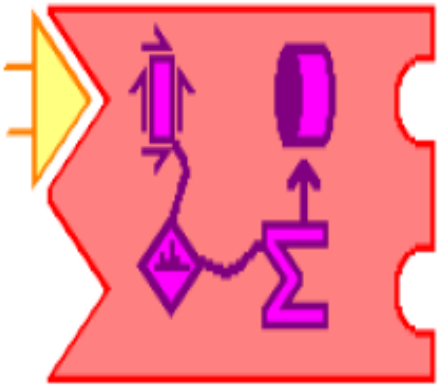


Hardware and Software Libraries legend:

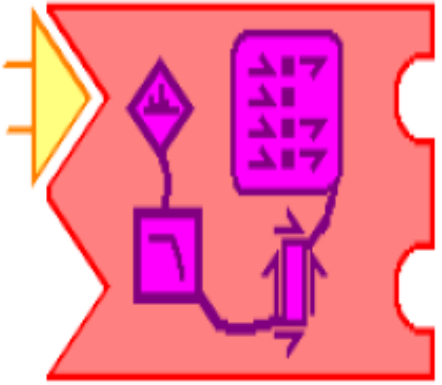


Applications

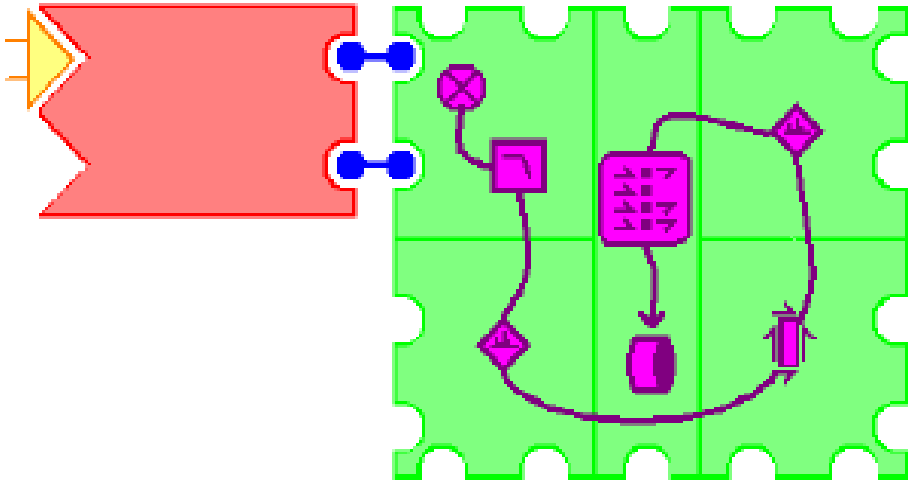
1) Pocket Spectrometer:



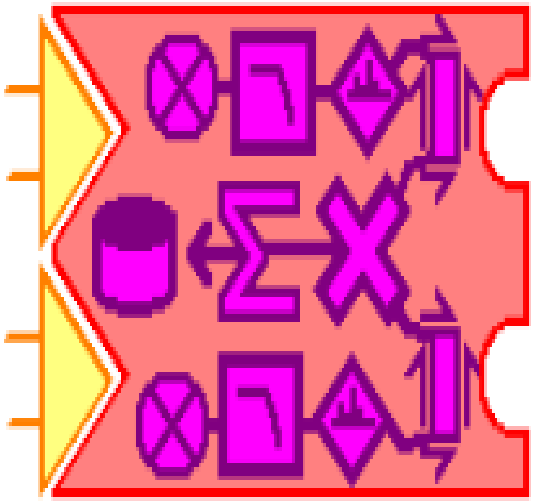
2) VLBI Channelizer:



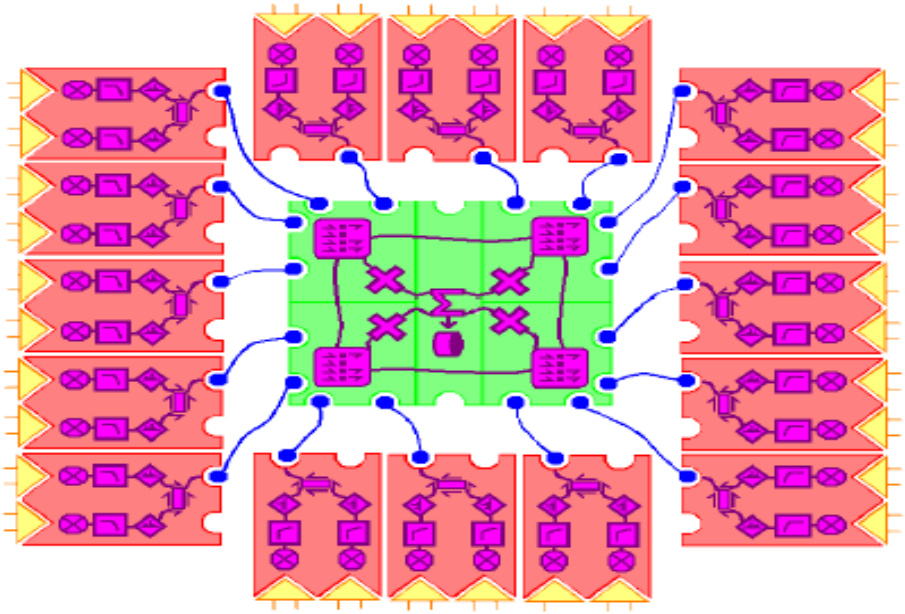
3) SETI Spectrometer:



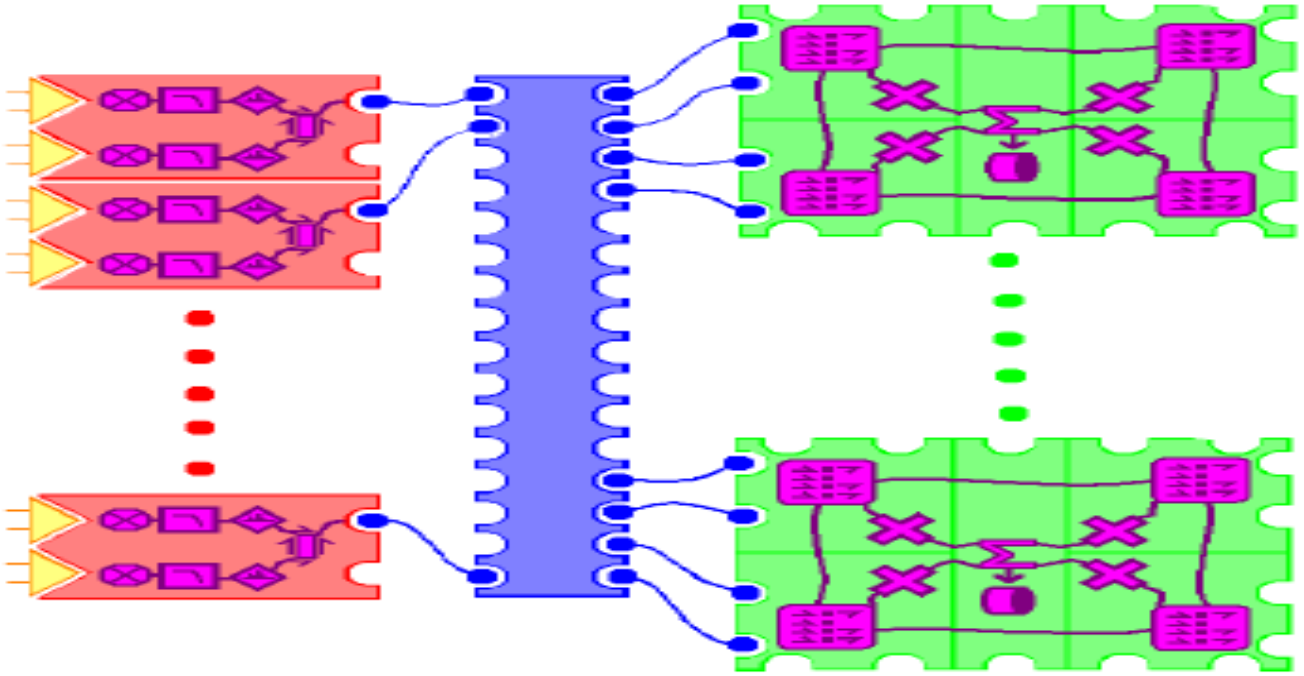
4) Pocket Correlator:



5) 32 Station Correlator:

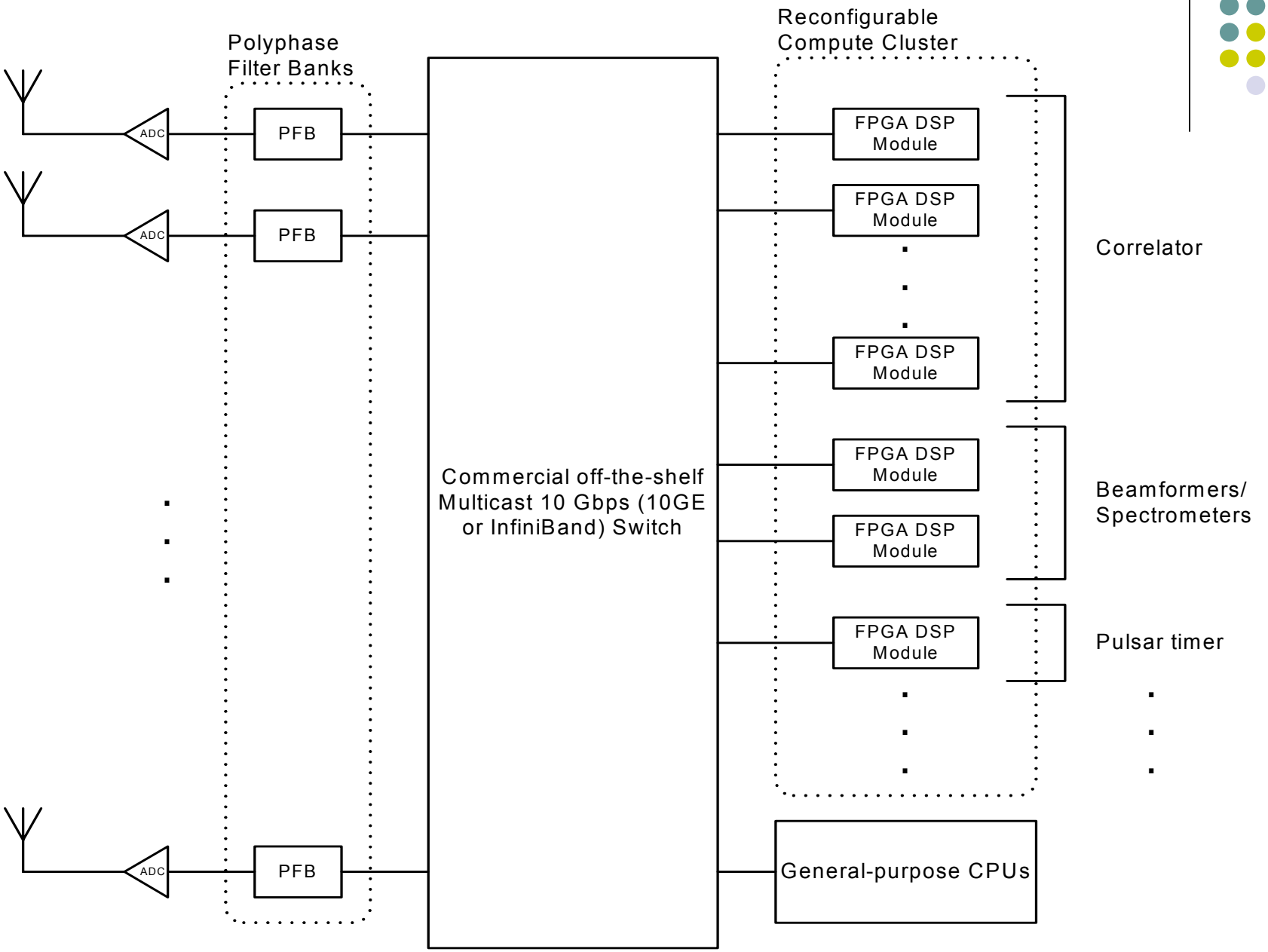


6) Arbitrary Sized Correlator



Beowulf Cluster Like General Purpose Architechture

Dynamic Allocation of Resources, need not be FPGA based



Applications

- VLBI Mark 5B data recorder – Haystack, NRAO – 512 MHz
- Beamforming – ATA, SMA –
- SETI – Arecibo (UCB)

  JPL/UCB DSN (Preston, Gulkis, Levin, Jones)
- Correlators and Imagers:

  ATA (Aaron Parsons, Mel Wright)

  PAPER (Reionization Experiment)

  Carma Next Gen

  MeerKAT/SKA South Africa

  GMRT next gen correlator ??

  Bologna (SKA), FASR ??

Pulsar Timing and Searching, Transient

Greenbank, Allen Telescope Array, VLA,

Swinburne (Parkes), meerKAT, Nancay

SETI Spectrometers

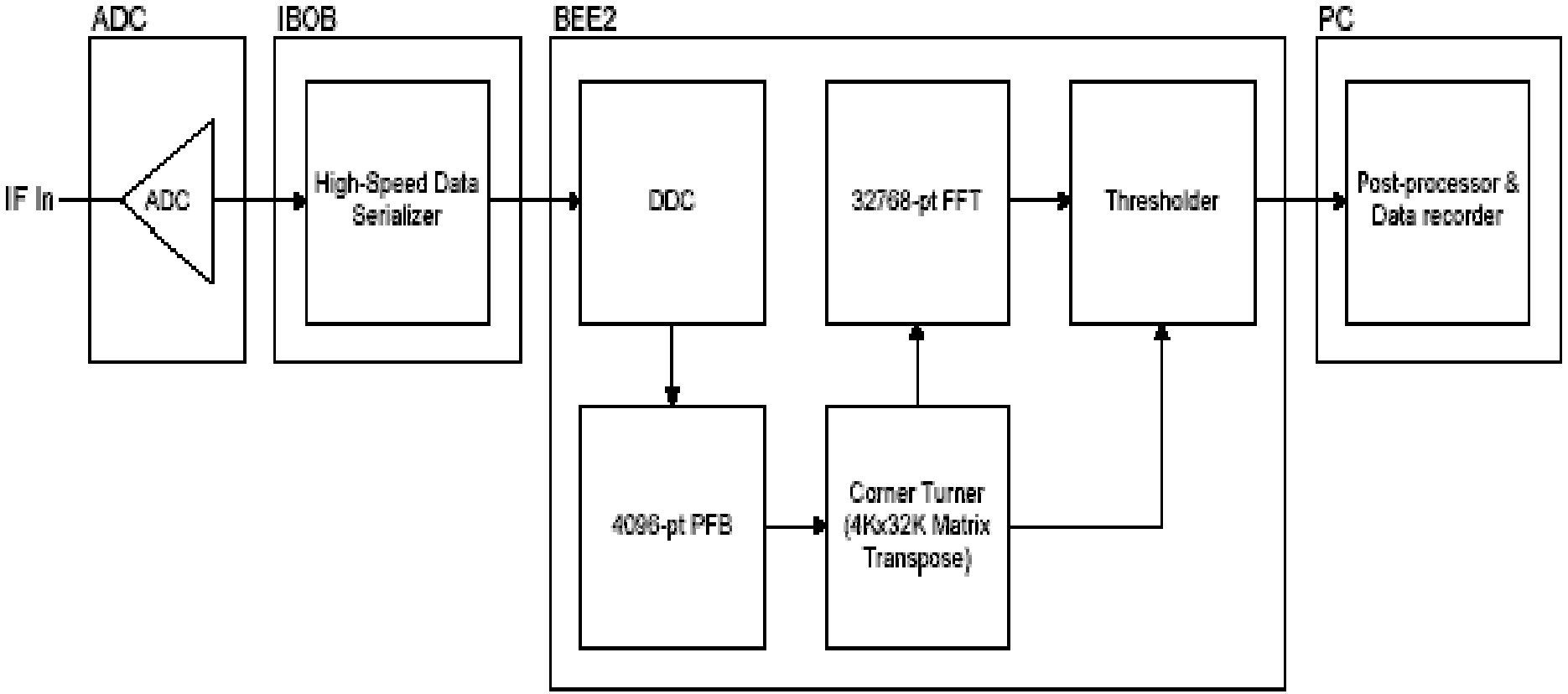
- Parkes Southern SERENDIP
- ALFA SETI Sky Survey (300 MHz x 7 beams)
- JPL DSN Sky Survey (eventually 20 GHz bandwidth)

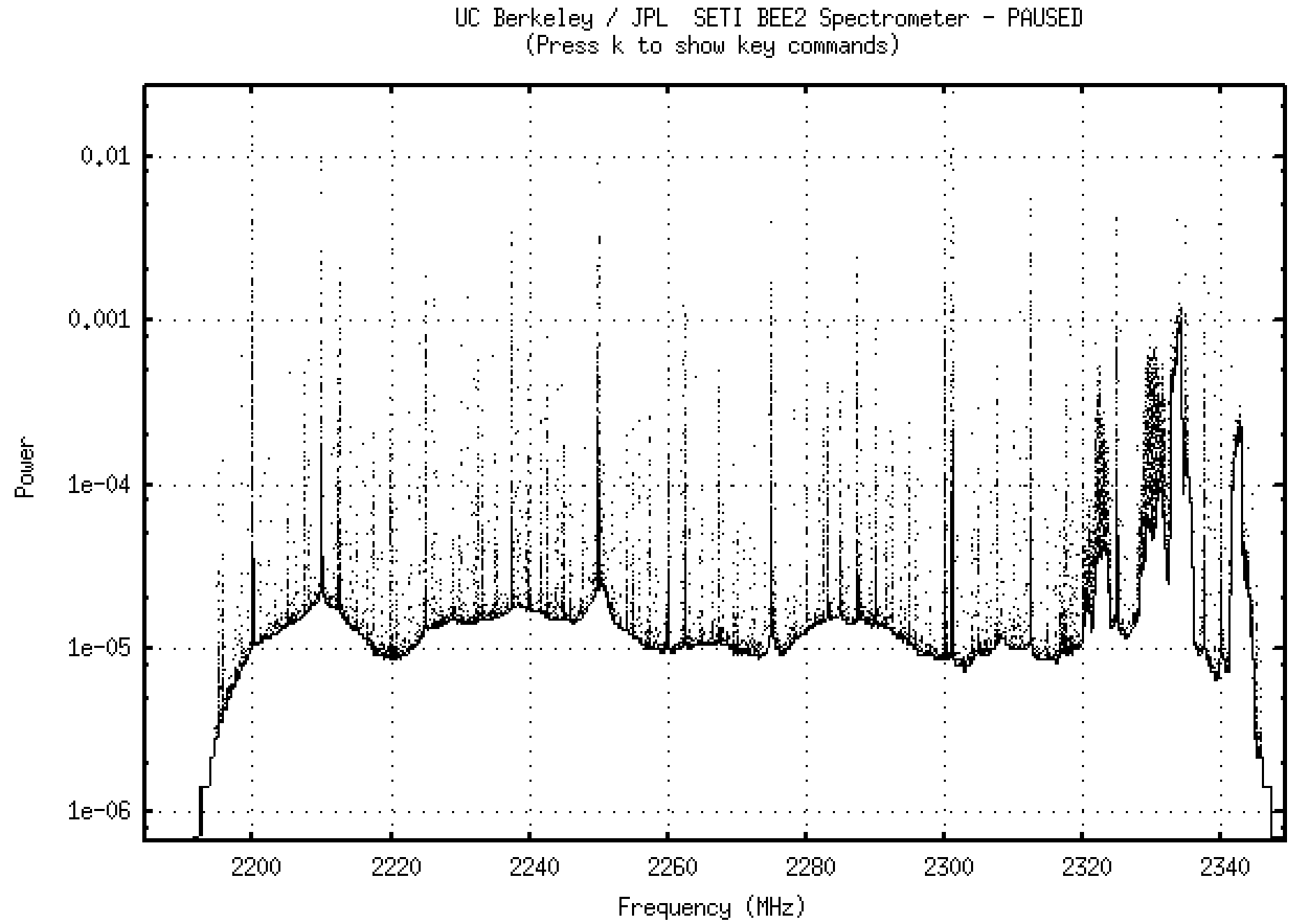
Radio Astronomy Spectrometers

- GALFA Spectrometer – Arecibo Multibeam Hydrogen Survey
- Astronomy Signal Processor – ASP – Don Backer, Ingrid Stairs, et al(pulsars)
- Antenna Holography, ATNF, China
- Gavert (DSN education, outreach)
- CMB Bolometer Readout – Caltech, UCB
- Fast Readout Spectrometers (Parkes, NRAO, ATA…)

128 Million Channel SETI Spectrometer

- 200 MHz Bandwidth, 2 Hz resolution

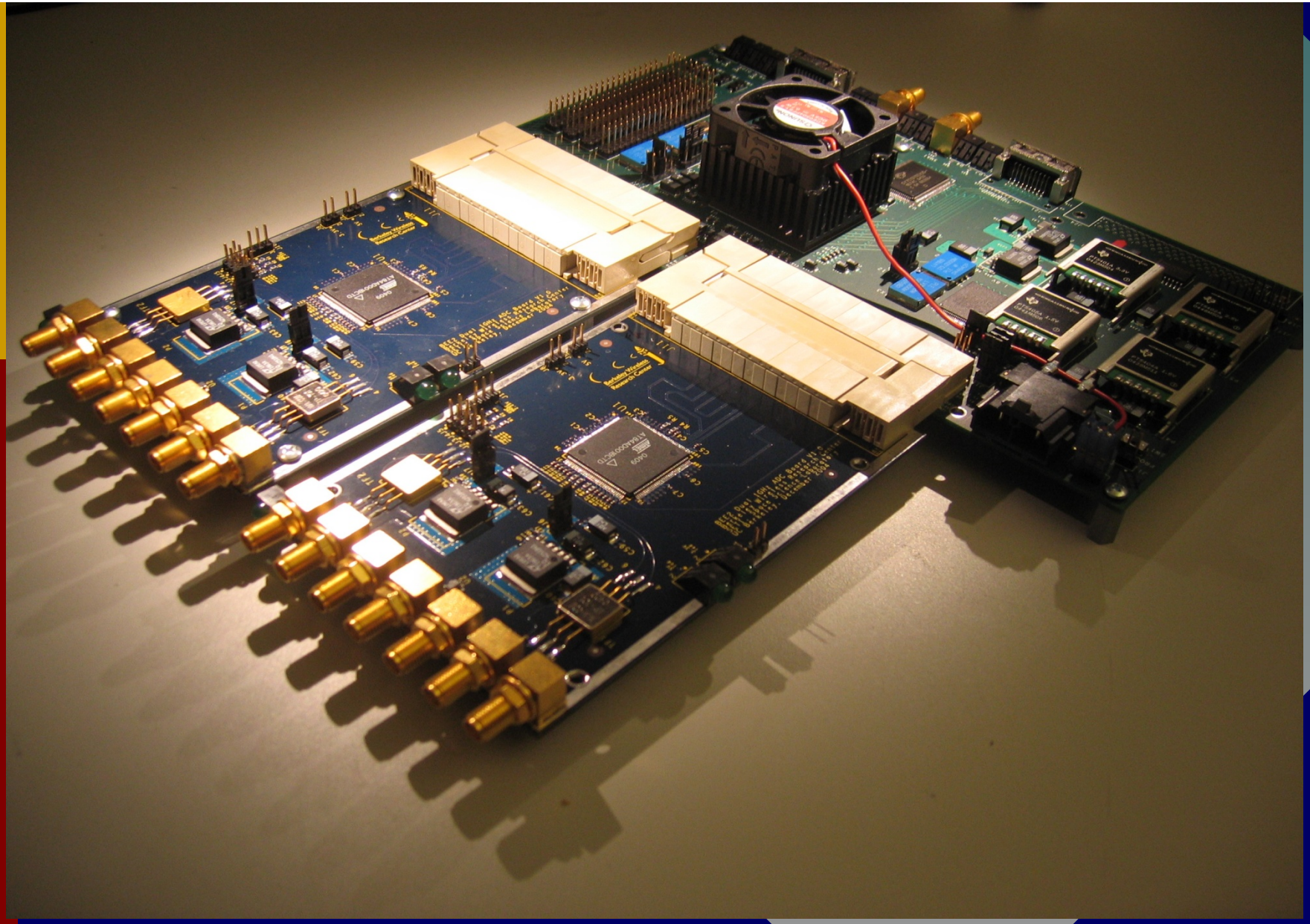




2353.86, 0.000626922

1 GHz bandwidth "Pocket Spectrometer"

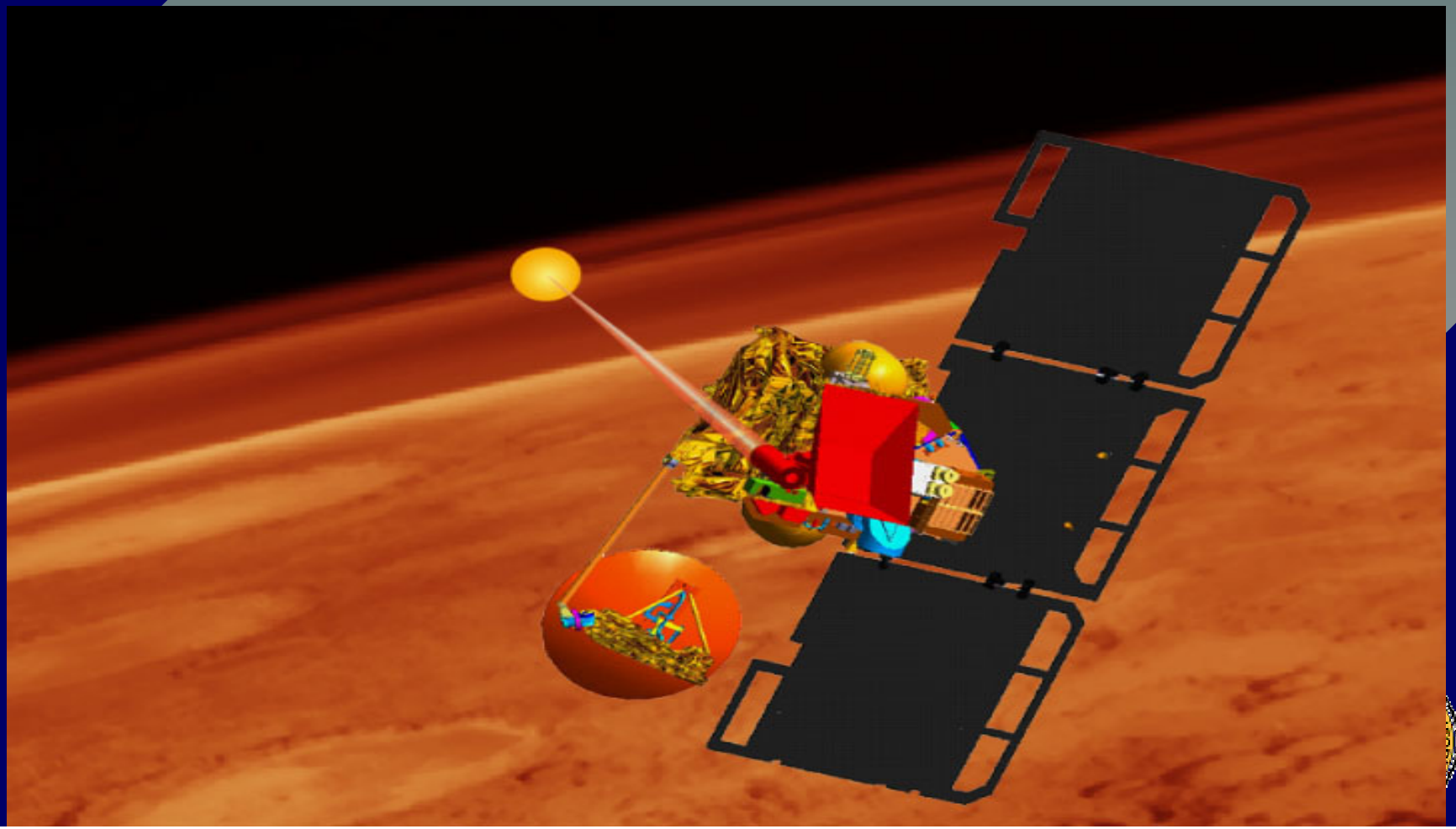
- Using ATMEL/E2V ADC's at 2 Gsamples/sec
- Performing 4 real FFT's in 1 (complex) biplex pipelined FFT module.
- 2048 channels
- Uses 1 ADC, 1 IBOB, and a laptop.



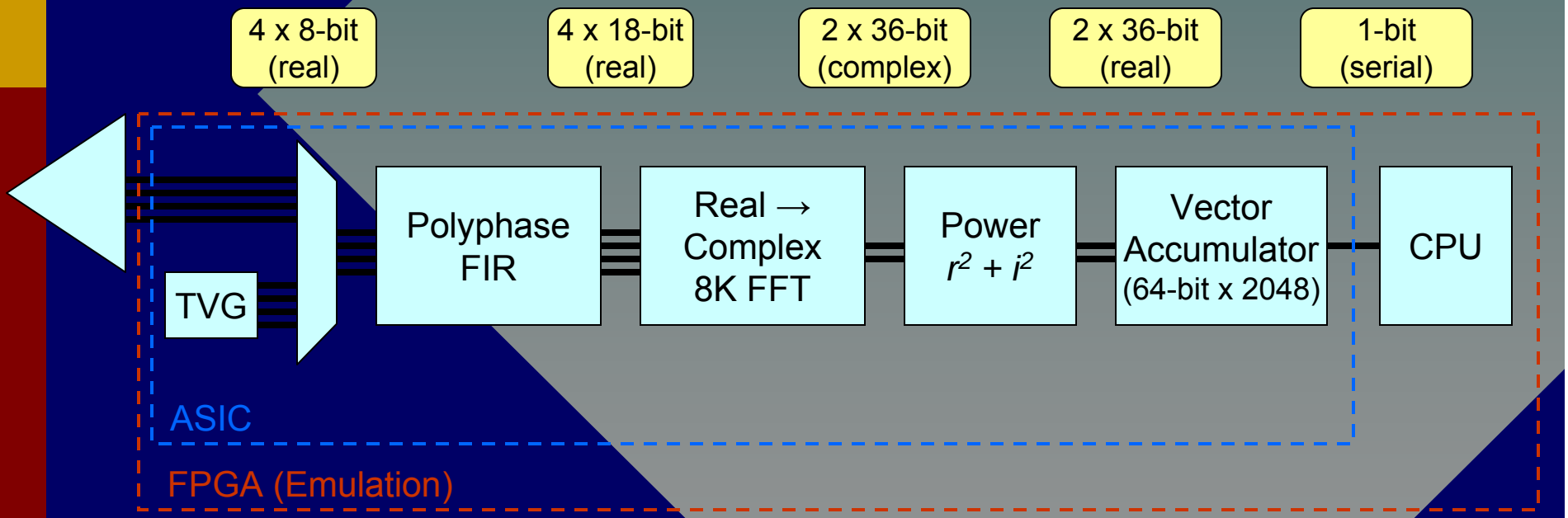
NASA MARVEL Mission:

Mars Volcanic Emission and Life Scout

sub-mm spectroscopy – water vents, methane, ??



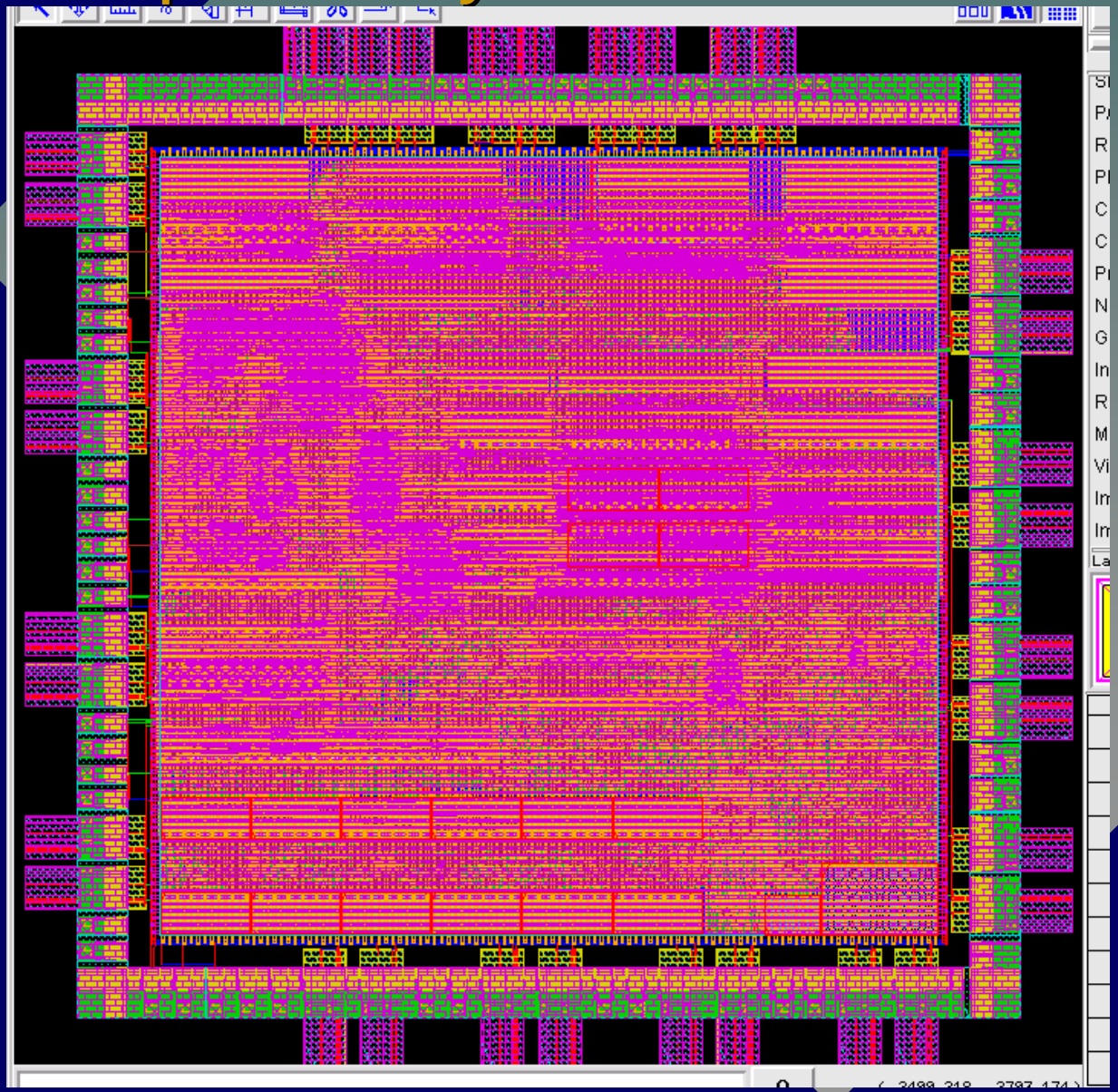
4096-Point Spectrometer



- Stream-based: 2K Packets
- Continuous operation

4096 channel Mars spectrometer

“Chip in a day” FPGA to ASIC

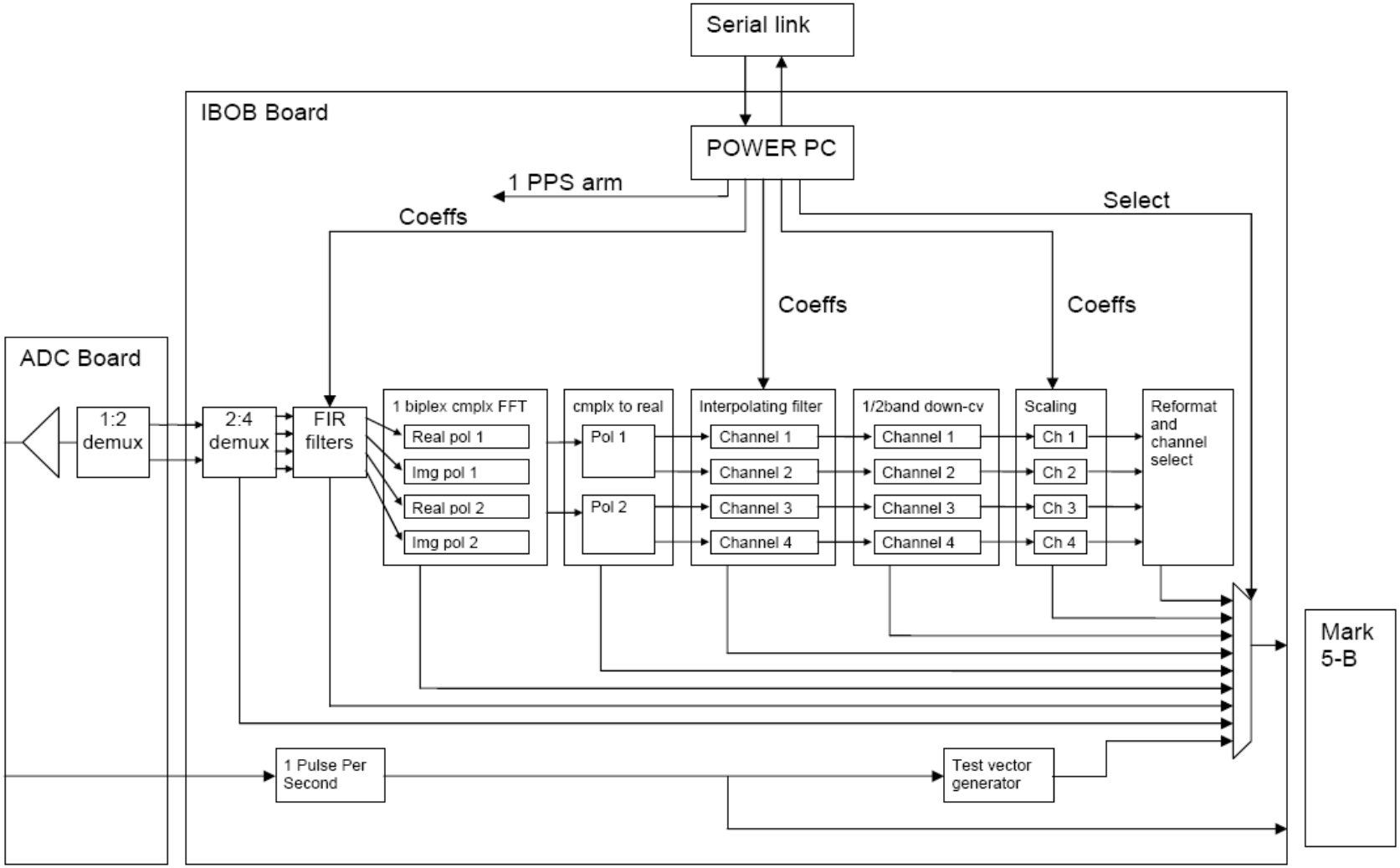


Portable VLBI backend – Henry Chen

- Interfaces to MARK 5B data recorder
- 500 MHz spectrum recorder.
- (This makes 4 instruments in 1 year!)

VLBI Mark 5B Front End

500 MHz BW, 32 channel filter bank



Pulsar/Transient Searching/Timing

NRAO, MeerKAT, Swinburne (Parkes), ATA

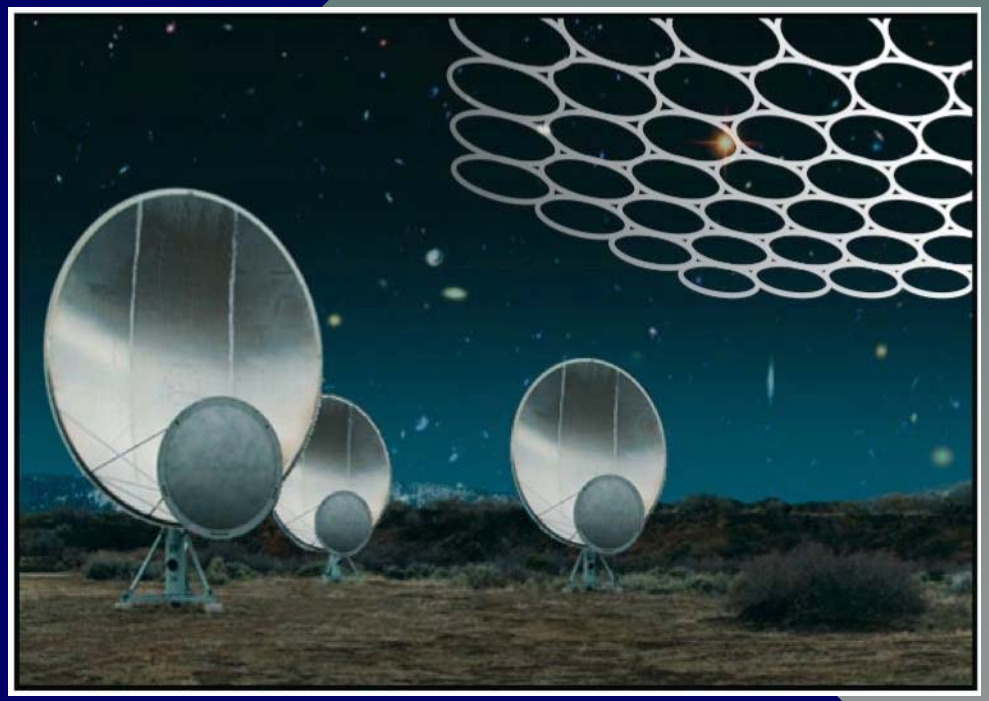
- 1 GHz bandwidth polyphase filter banks

  1024 channels, 30 uS readout , full stokes

  (Parkes = 300 MHz * 7 beams)

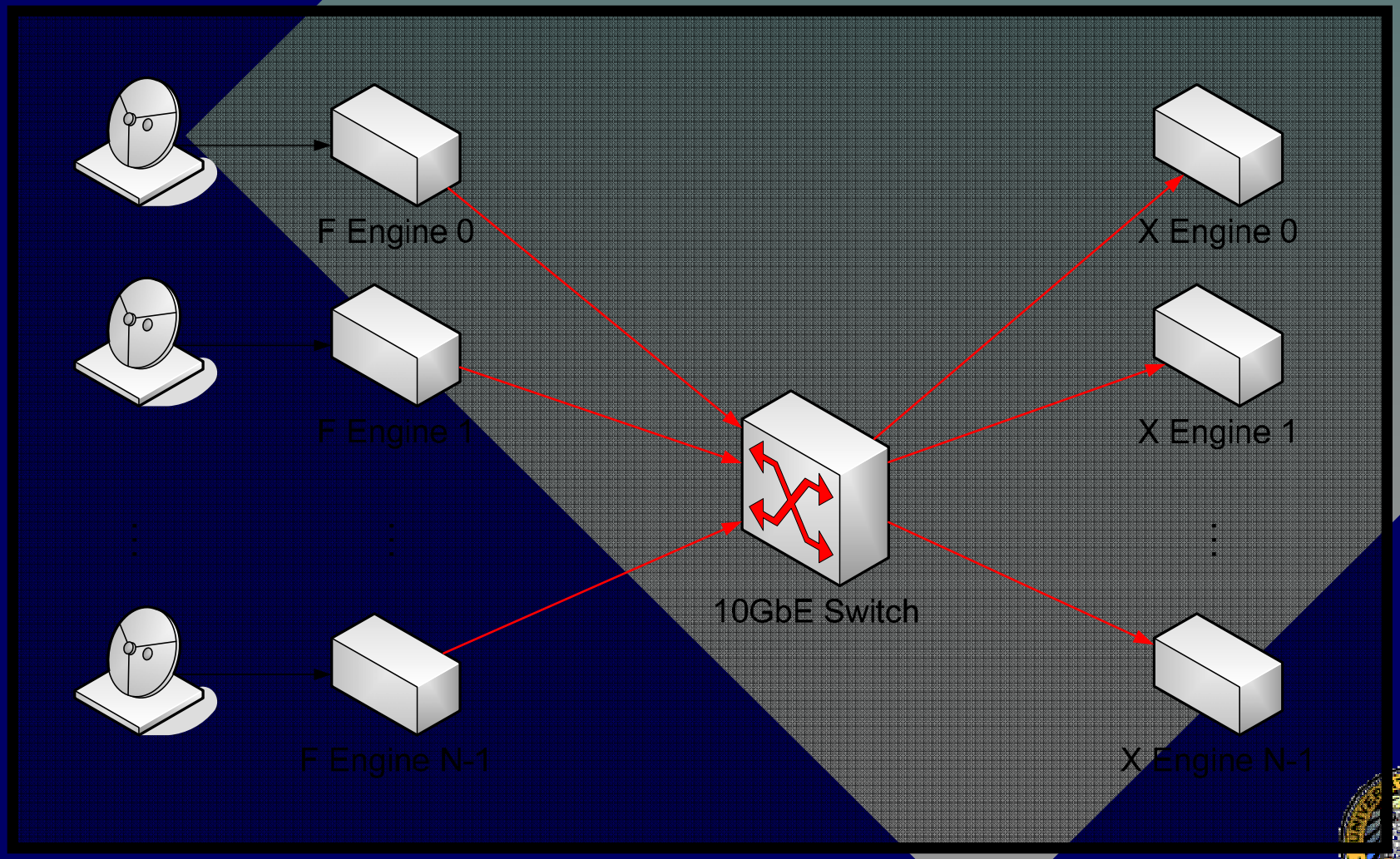
- 1 GHz coherent dedispersion (PFB, FFT, FFT^{-1})

ATA Fly's Eye Transient Instrument
44 fast readout spectrometers
3 weeks to build



Geoff Bower, Jim Cordes, Griffin Foster, Joeri van Leeuwen, Peter McMahon, Andrew Siemion, Mark Wagner, Dan Werthimer

CASPER FX Architecture

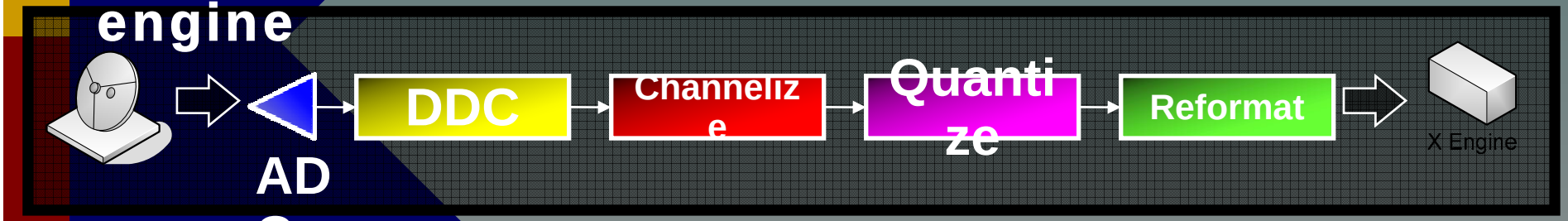


Correlators and Beamformers

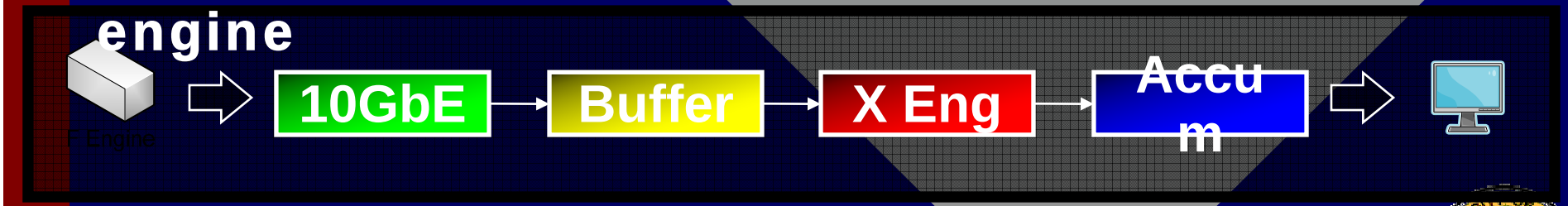
- Globally Asynchronous (like a computer cluster)
- Data is time stamped with 1 PPS at ADC
- Locally Synchronous, Globally Asynchronous
- Solve problem of correlator/beamformer interconnect problem by using 10 Gbe switches (for both interconnect and fast readout)
- No need for high density complex boards
- Use Fifo's to align data before correlation or beamforming...

Engine Operations

F engine



X engine



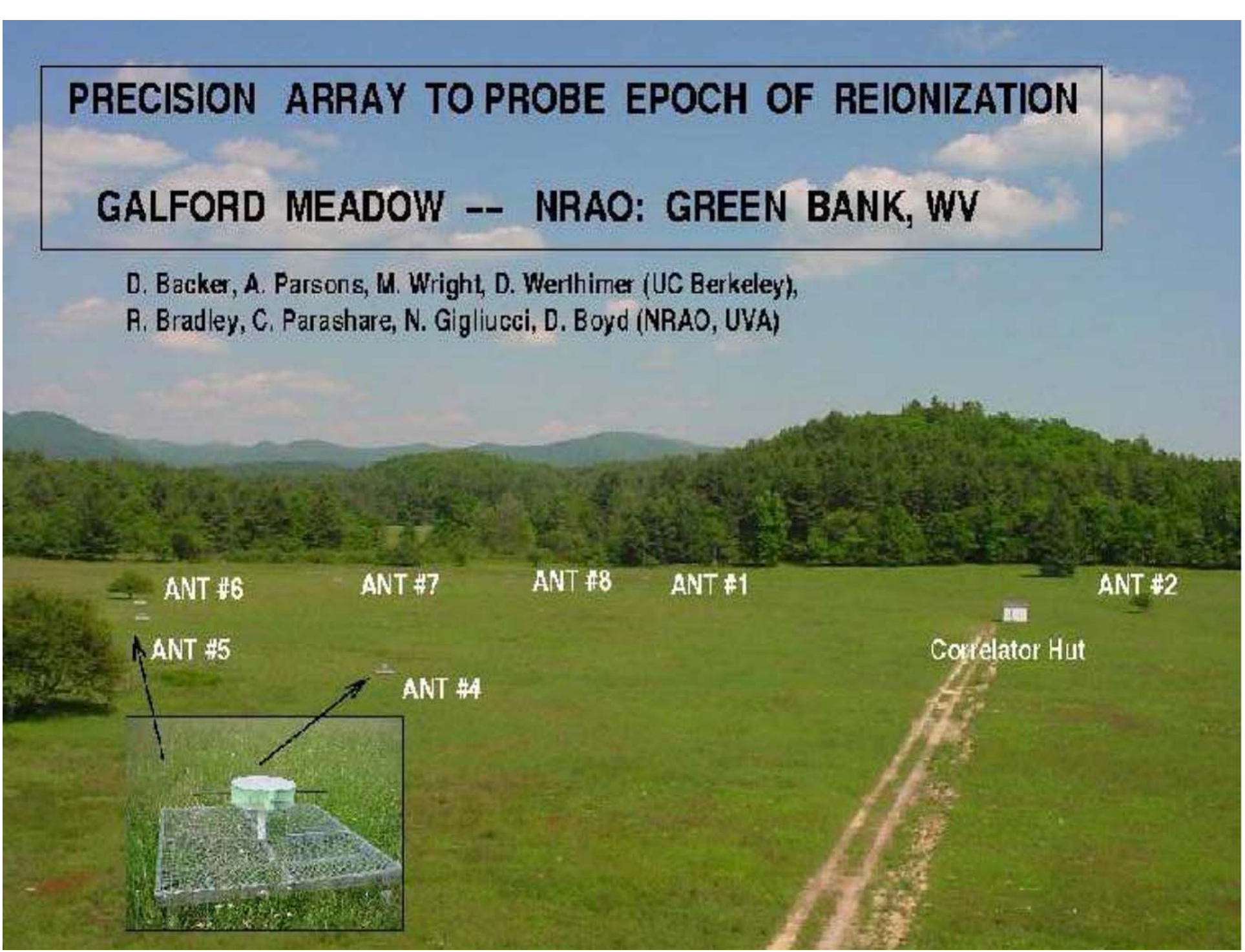

Experiment in Progress
DO NOT TOUCH
Contact
LAB BENCH #13

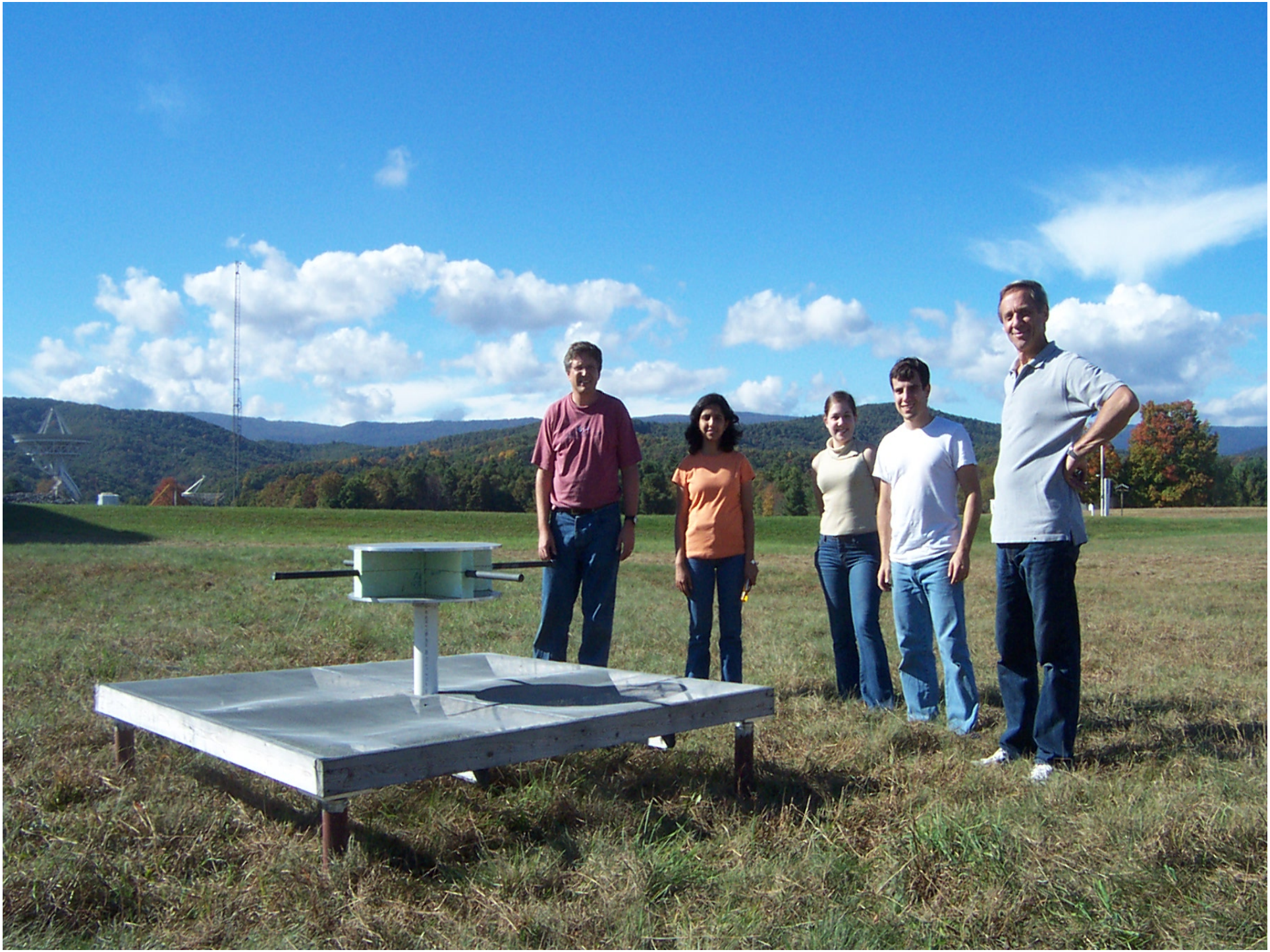

Cal
UC BERKELEY

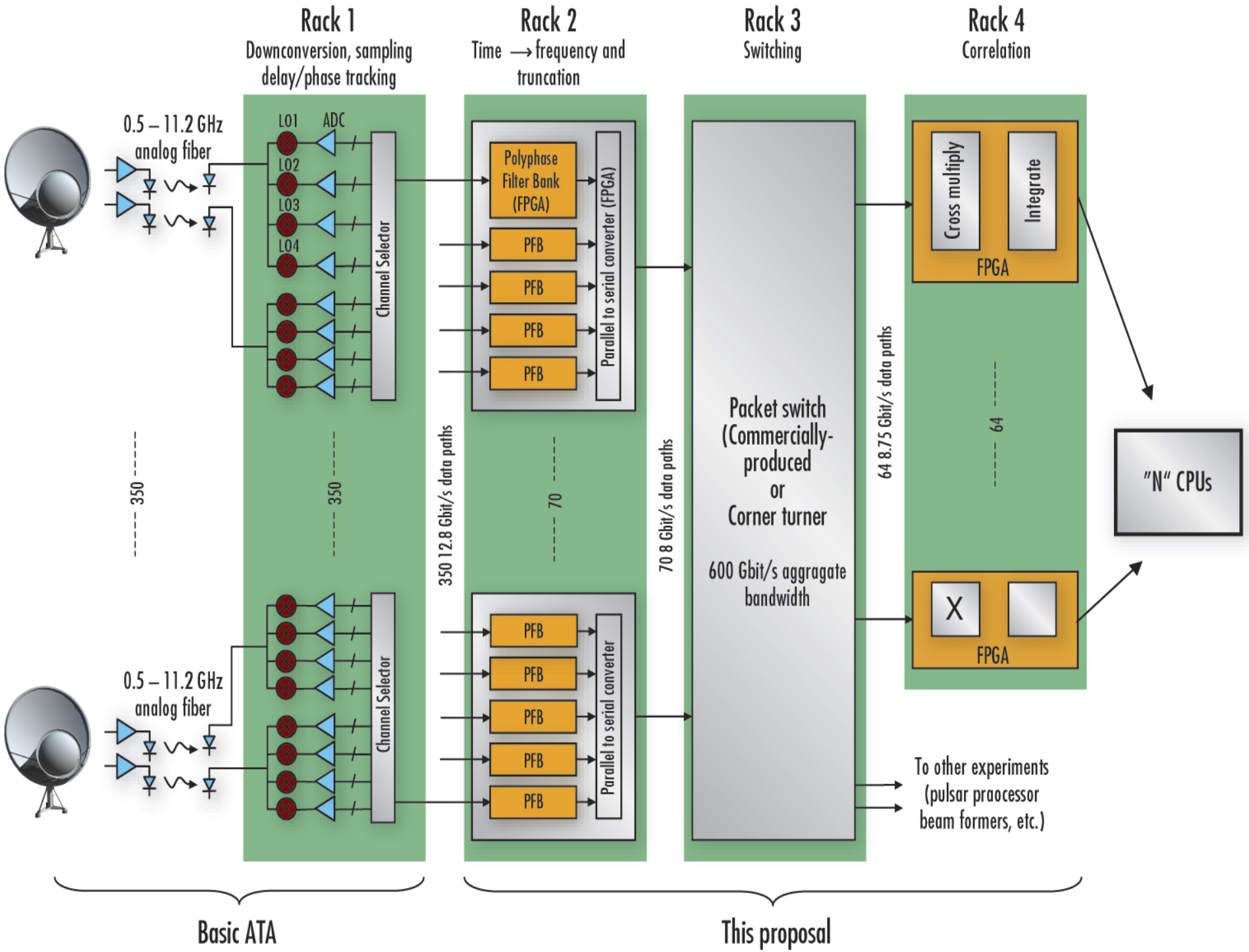
PRECISION ARRAY TO PROBE EPOCH OF REIONIZATION

GALFORD MEADOW -- NRAO: GREEN BANK, WV

D. Backer, A. Parsons, M. Wright, D. Werthimer (UC Berkeley),
R. Bradley, C. Parashare, N. Gigliucci, D. Boyd (NRAO, UVA)






Rack 1
Downconversion, sampling delay/phase tracking
Rack 2
Time → frequency and truncation
Rack 3
Switching
Rack 4
Correlation
0.5 – 11.2 GHz analog fiber
LO1
LO2
LO3
LO4
ADC
Channel Selector
350
350
350 12.8 Gbit/s data paths
Polyphase Filter Bank (FPGA)
PFB
PFB
PFB
PFB
Parallel to serial converter (FPGA)
70
70 8 Gbit/s data paths
Packet switch (Commercially-produced or Corner turner
600 Gbit/s aggregate bandwidth
64 8.75 Gbit/s data paths
Cross multiply
Integrate
FPGA
64
"N" CPUs
0.5 – 11.2 GHz analog fiber
Channel Selector
PFB
PFB
PFB
PFB
Parallel to serial converter
X
FPGA
To other experiments (pulsar praocessor beam formers, etc.)
Basic ATA
This proposal

Digital Correlator Costs - 2008

cost = bandwidth/GHz * [(Nant * $4000) + ($Nant^2$ * $50)]

where Nant = number of dual pol antenna (full stokes correlator)
for single pol correlator, use Nant/2

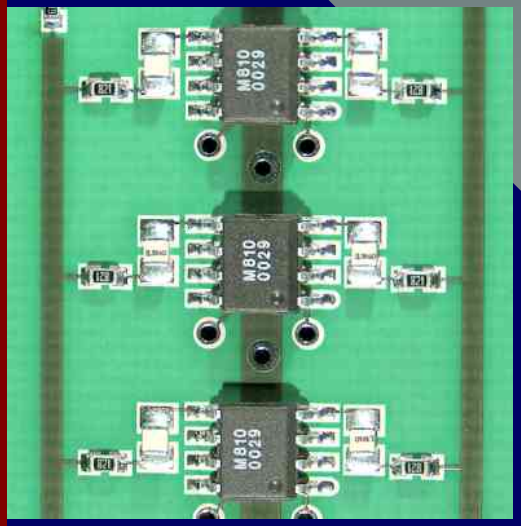
Nchannels = 16,384 (cost goes with log(Nchannels)

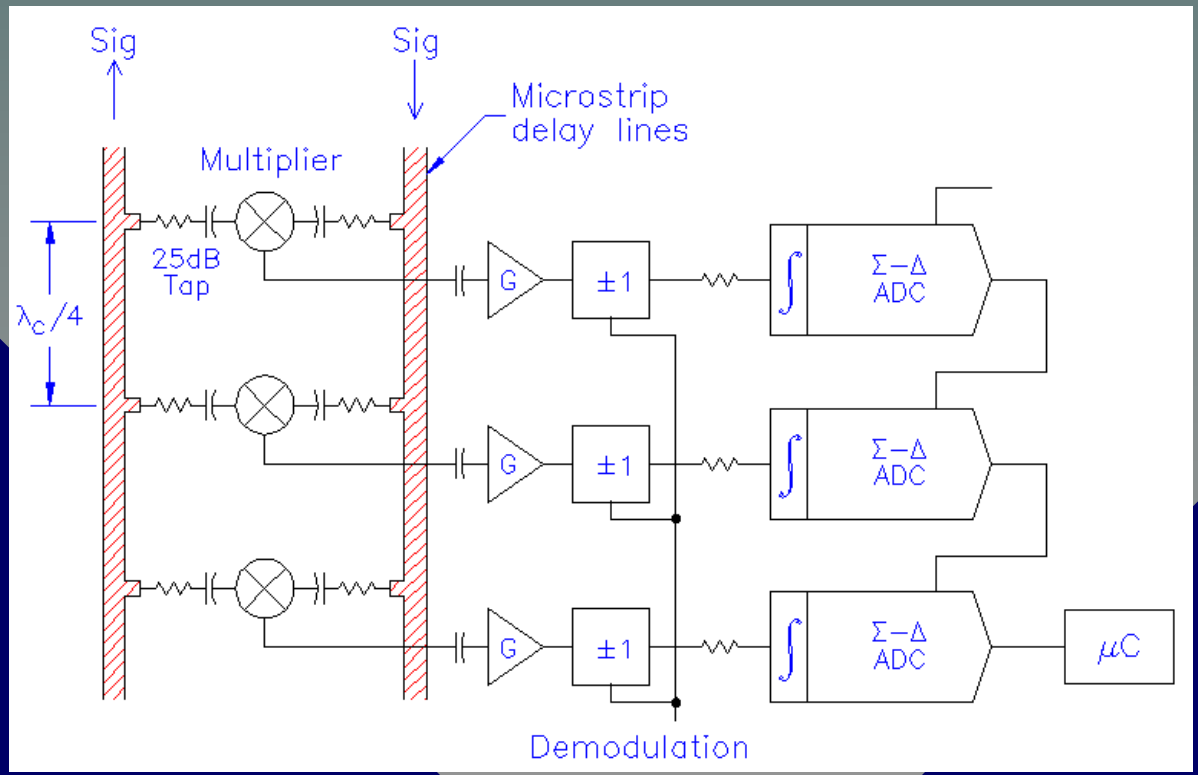
Cost goes down by two every 1.5 years

\

Analog Correlator- Andy Harris

$$S_{xy}(f) \leftrightarrow R_{xy}(\tau) \qquad R_{xy}(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} V_x(t) \times V_y(t+\tau)\, dt$$





Wideband, simple analog electronics: low-speed digitization and signal processing *after* high frequency delay and multiplication

Digital Spectrometer Costs - 2008

cost = $1 / MHz

Nchannels = 16,384 (cost goes with log(Nchannels)

Cost goes down by two every 1.5 years

\

2008 Parts Costs (list prices, Q=100)

$1 per MHz per beam per polarization:

Atmel AT84AD001 ADC = $100

Xilinx Virtex 5 FPGA = $ 500

PCB and misc parts, assembly = $400

Cost = $1 * Bandwidth/MHz * Log2(Nchannels/16384)

University discounts? Donated Chips?

ADC's

- 2 Gsps, or dual 1 Gsps, 8 bit, E2V, $100
- 3 Gsps, 8 bit, National, can be interleaved FOR 6 Gsps
- 5 Gsps, dual 2.5 Gsps, or quad 1.25, 8 bit, E2V
- 8 to 10 Gsps – three companies will announce
- 20 Gsps, 8 bit, Agilent – not for sale

  (can be interleaved for 40 Gsps, 13 GHz BW)

  80 Gsps coming

  Inphi, Others….

Agilent ADC-FGPA-CX4 board ?

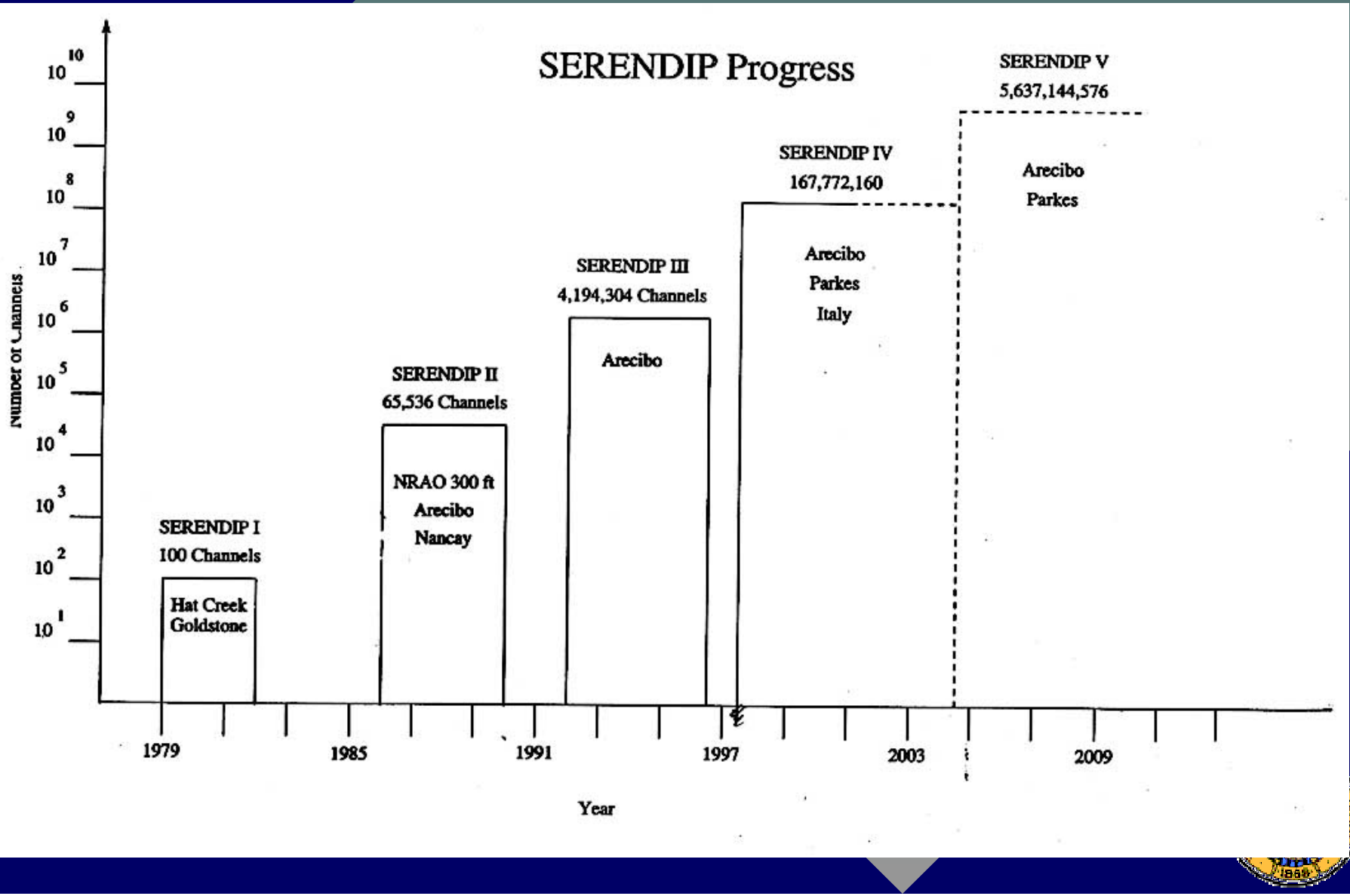
20 Gsps 8 bit Agilent ADC

XC5VSX240T

6 CX4 ports

120 Gbps xaui
100 Gbps infiniband
60 Gbps 10 Gbe

Moores Law – Instruments using FPGA's: 2X per year (1,000,000 over 20 years)



Future Spectrometers

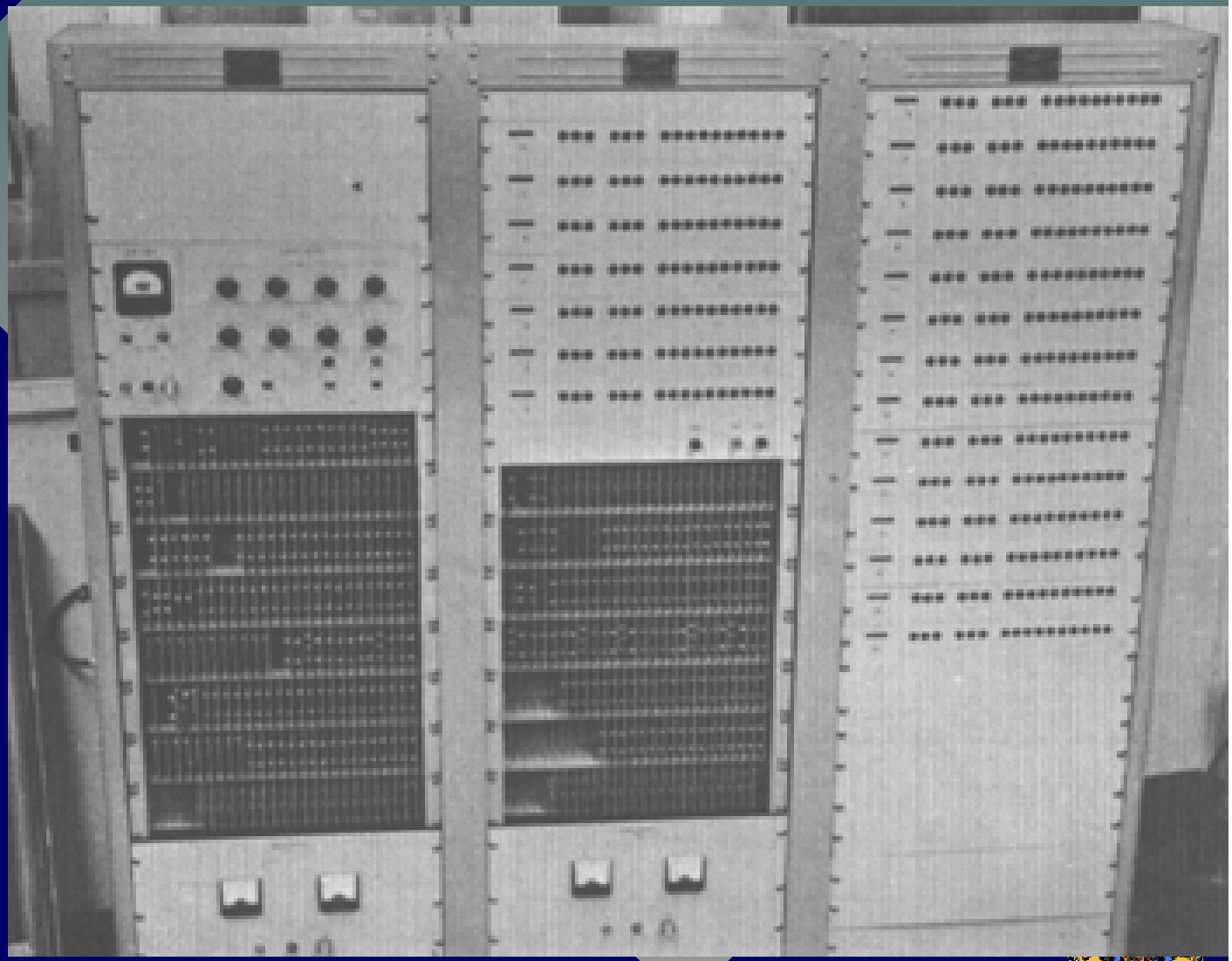
2015	4 THz	400 beams 10 GHz each
2020	128 THz	12,800 beams
2025	4000 THz	40,000 beams
2030	128,000 THz	1M beams

1960 – First Radio Astronomy Digital Correlator

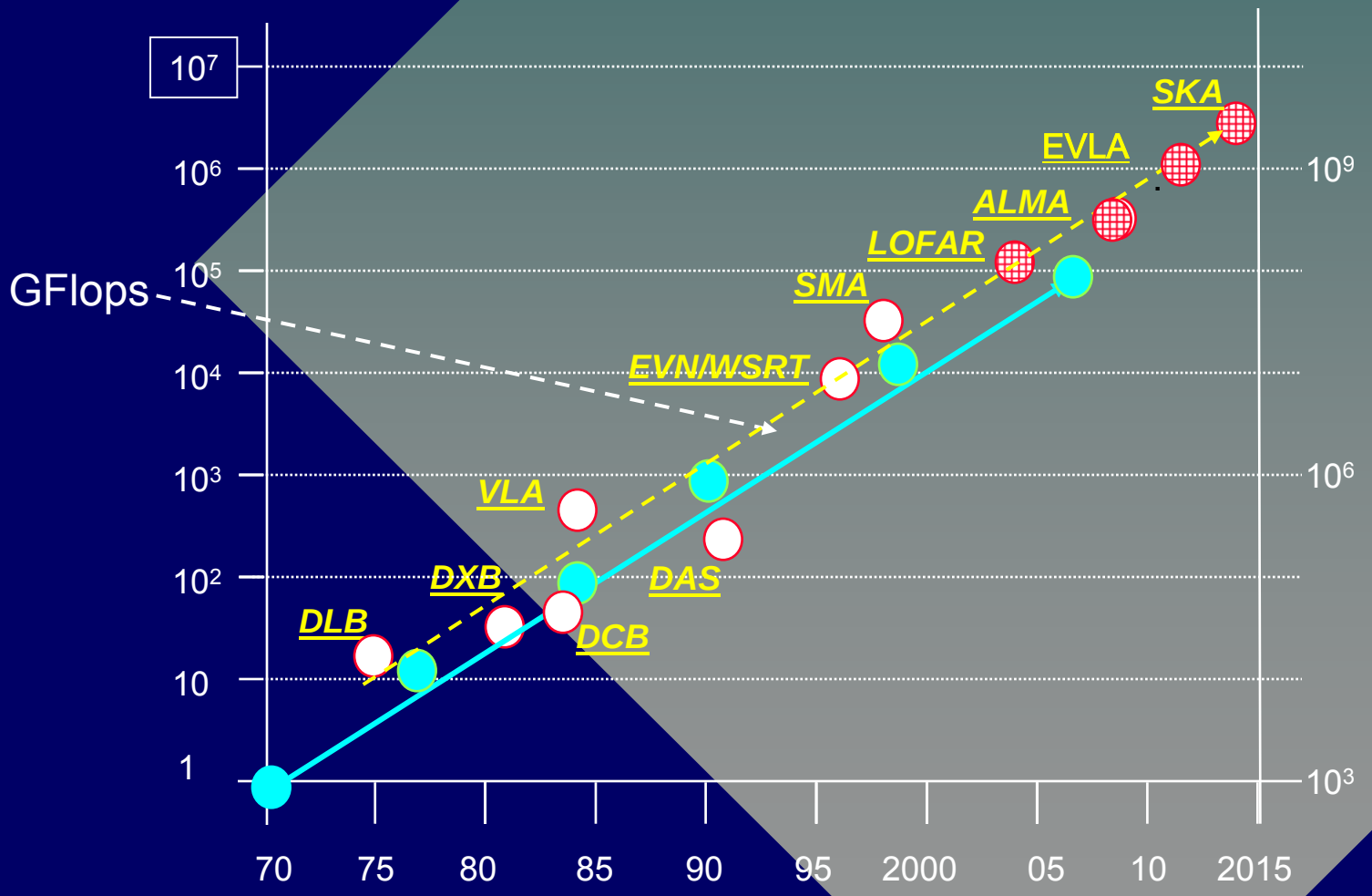
21 lags
300kHz clock
discrete transistors

$19,000

Sandy Weinreb



Correlator processing power



source: Arnold van Ardenne

Selected correlator quotes

Sandy Weinreb

"In 1960 there were no chips; just discrete transistors! The $19,000 was the cost of the samplers, shift registers, and counter. It did not include the cost of the 21 accumulators which I made myself in a few months getting paid $240/month."

Ray Escoffier

"With correlator performance having gone up by a factor of 922,000 over the last 30 years, its only fair that correlator design engineers' salaries should have gone up by a similar factor!!"

Sergei Pogrebenko

"It is desirable that the output data rate from a data processor is less than the input data rate."

Ray Escoffier

"With correlator performance having gone up by a factor of 922,000 over the last 30 years, its only fair that correlator design engineers' salaries should have gone up by a similar factor!!"

CASPER the Friendly…

- Group Helping Open-source Signal-processing Technology (GHOST?)
  - Goal to help develop signal processing instrumenation and libraries for the community.
  - Open source hardware, gateware, and software.
  - Provide training and tutorials
  - Not so much delivering turn-key instruments
  - Promote Collaboration

Collaboration (not turn key instruments)

- Share Open Source Libraries
- Workshops (Tamara)
- Video's and Doc's on Tool Flow, Libraries
- Wiki, Mailing List
- Open Source Boards (available from vendors)

MOVIE!!! (9X speed up)

- Building Spectrometer
- Correlator